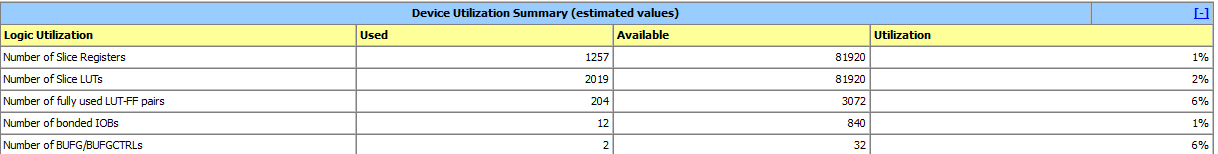
# 1024x768, 32x32 Kreuz mit Kreis



Started : "Synthesize - XST".

Running xst...

Command Line: xst -intstyle ise -ifn "C:/Users/frank.schumacher/Merses/Work/VHDL/Correlation\_ShiftPipeline15052012/Houghtransform.xst" -ofn "C:/Users/frank.schumacher/Merses/Work/VHDL/Correlation\_ShiftPipeline15052012/Houghtransform.syr"

Reading design: Houghtransform.prj

=========================================================================

\* HDL Compilation \*

=========================================================================

Compiling vhdl file "C:/Users/frank.schumacher/Merses/Work/VHDL/Correlation\_ShiftPipeline15052012/source/imagedata.vhd" in Library work.

Compiling vhdl file "C:/Users/frank.schumacher/Merses/Work/VHDL/Correlation\_ShiftPipeline15052012/source/maskdata.vhd" in Library work.

Package <maskdata> compiled.

Compiling vhdl file "C:/Users/frank.schumacher/Merses/Work/VHDL/Correlation\_ShiftPipeline15052012/source/referencedata.vhd" in Library work.

Package <referencedata> compiled.

Compiling vhdl file "C:/Users/frank.schumacher/Merses/Work/VHDL/Correlation\_ShiftPipeline15052012/source/topx0.vhd" in Library work.

Architecture behavioral of Entity houghtransform is up to date.

=========================================================================

\* Design Hierarchy Analysis \*

=========================================================================

Analyzing hierarchy for entity <Houghtransform> in library <work> (architecture <behavioral>).

=========================================================================

\* HDL Analysis \*

=========================================================================

Analyzing Entity <Houghtransform> in library <work> (Architecture <behavioral>).

Entity <Houghtransform> analyzed. Unit <Houghtransform> generated.

=========================================================================

\* HDL Synthesis \*

=========================================================================

Performing bidirectional port resolution...

Synthesizing Unit <Houghtransform>.

Related source file is "C:/Users/frank.schumacher/Merses/Work/VHDL/Correlation\_ShiftPipeline15052012/source/topx0.vhd".

WARNING:Xst:1780 - Signal <pixOut\_sig\_next> is never used or assigned. This unconnected signal will be trimmed during the optimization process.

WARNING:Xst:646 - Signal <delayPipeline<0><0>> is assigned but never used. This unconnected signal will be trimmed during the optimization process.

Found 8-bit register for signal <pixOut>.

.

Found 31775-bit register for signal <delayPipeline<1:31775>> Found 8-bit adder for signal <pixOut\_sig>.

Found 8-bit adder for signal <pixOut\_sig$addsub0000> created at line 64.

Found 8-bit adder for signal <pixOut\_sig$addsub0001> created at line 64.

Found 8-bit adder for signal <pixOut\_sig$addsub0002> created at line 64.

Found 8-bit adder for signal <pixOut\_sig$addsub0003> created at line 64.

Found 8-bit adder for signal <sum$add0000> created at line 64.

Found 8-bit adder for signal <sum$add0001> created at line 64.

Found 8-bit adder for signal <sum$add0002> created at line 64.

Found 8-bit adder for signal <sum$add0003> created at line 64.

Found 8-bit adder for signal <sum$add0004> created at line 64.

Found 8-bit adder for signal <sum$add0005> created at line 64.

Found 8-bit adder for signal <sum$add0006> created at line 64.

Found 8-bit adder for signal <sum$add0007> created at line 64.

Found 8-bit adder for signal <sum$add0008> created at line 64.

Found 8-bit adder for signal <sum$add0009> created at line 64.

Found 8-bit adder for signal <sum$add0010> created at line 64.

Found 8-bit adder for signal <sum$add0011> created at line 64.

Found 8-bit adder for signal <sum$add0012> created at line 64.

Found 8-bit adder for signal <sum$addsub0000> created at line 64.

Found 8-bit adder for signal <sum$addsub0001> created at line 64.

Found 8-bit adder for signal <sum$addsub0002> created at line 64.

Found 8-bit adder for signal <sum$addsub0003> created at line 64.

Found 8-bit adder for signal <sum$addsub0004> created at line 64.

Found 8-bit adder for signal <sum$addsub0005> created at line 64.

Found 8-bit adder for signal <sum$addsub0006> created at line 64.

Found 8-bit adder for signal <sum$addsub0007> created at line 64.

Found 8-bit adder for signal <sum$addsub0008> created at line 64.

Found 8-bit adder for signal <sum$addsub0009> created at line 64.

Found 8-bit adder for signal <sum$addsub0010> created at line 64.

Found 8-bit adder for signal <sum$addsub0011> created at line 64.

Found 8-bit adder for signal <sum$addsub0012> created at line 64.

Found 8-bit adder for signal <sum$addsub0013> created at line 64.

Found 8-bit adder for signal <sum$addsub0014> created at line 64.

Found 8-bit adder for signal <sum$addsub0015> created at line 64.

Found 8-bit adder for signal <sum$addsub0016> created at line 64.

Found 8-bit adder for signal <sum$addsub0017> created at line 64.

Found 8-bit adder for signal <sum$addsub0018> created at line 64.

Found 8-bit adder for signal <sum$addsub0019> created at line 64.

Found 8-bit adder for signal <sum$addsub0020> created at line 64.

Found 8-bit adder for signal <sum$addsub0021> created at line 64.

Found 8-bit adder for signal <sum$addsub0022> created at line 64.

Found 8-bit adder for signal <sum$addsub0023> created at line 64.

Found 8-bit adder for signal <sum$addsub0024> created at line 64.

Found 8-bit adder for signal <sum$addsub0025> created at line 64.

Found 8-bit adder for signal <sum$addsub0026> created at line 64.

Found 8-bit adder for signal <sum$addsub0027> created at line 64.

Found 8-bit adder for signal <sum$addsub0028> created at line 64.

Found 8-bit adder for signal <sum$addsub0029> created at line 64.

Found 8-bit adder for signal <sum$addsub0030> created at line 64.

Found 8-bit adder for signal <sum$addsub0031> created at line 64.

Found 8-bit adder for signal <sum$addsub0032> created at line 64.

Found 8-bit adder for signal <sum$addsub0033> created at line 64.

Found 8-bit adder for signal <sum$addsub0034> created at line 64.

Found 8-bit adder for signal <sum$addsub0035> created at line 64.

Found 8-bit adder for signal <sum$addsub0036> created at line 64.

Found 8-bit adder for signal <sum$addsub0037> created at line 64.

Found 8-bit adder for signal <sum$addsub0038> created at line 64.

Found 8-bit adder for signal <sum$addsub0039> created at line 64.

Found 8-bit adder for signal <sum$addsub0040> created at line 64.

Found 8-bit adder for signal <sum$addsub0041> created at line 64.

Found 8-bit adder for signal <sum$addsub0042> created at line 64.

Found 8-bit adder for signal <sum$addsub0043> created at line 64.

Found 8-bit adder for signal <sum$addsub0044> created at line 64.

Found 8-bit adder for signal <sum$addsub0045> created at line 64.

Found 8-bit adder for signal <sum$addsub0046> created at line 64.

Found 8-bit adder for signal <sum$addsub0047> created at line 64.

Found 8-bit adder for signal <sum$addsub0048> created at line 64.

Found 8-bit adder for signal <sum$addsub0049> created at line 64.

Found 8-bit adder for signal <sum$addsub0050> created at line 64.

Found 8-bit adder for signal <sum$addsub0051> created at line 64.

Found 8-bit adder for signal <sum$addsub0052> created at line 64.

Found 8-bit adder for signal <sum$addsub0053> created at line 64.

Found 8-bit adder for signal <sum$addsub0054> created at line 64.

Found 8-bit adder for signal <sum$addsub0055> created at line 64.

Found 8-bit adder for signal <sum$addsub0056> created at line 64.

Found 8-bit adder for signal <sum$addsub0057> created at line 64.

Found 8-bit adder for signal <sum$addsub0058> created at line 64.

Found 8-bit adder for signal <sum$addsub0059> created at line 64.

Found 8-bit adder for signal <sum$addsub0060> created at line 64.

Found 8-bit adder for signal <sum$addsub0061> created at line 64.

Found 8-bit adder for signal <sum$addsub0062> created at line 64.

Found 8-bit adder for signal <sum$addsub0063> created at line 64.

Found 8-bit adder for signal <sum$addsub0064> created at line 64.

Found 8-bit adder for signal <sum$addsub0065> created at line 64.

Found 8-bit adder for signal <sum$addsub0066> created at line 64.

Found 8-bit adder for signal <sum$addsub0067> created at line 64.

Found 8-bit adder for signal <sum$addsub0068> created at line 64.

Found 8-bit adder for signal <sum$addsub0069> created at line 64.

Found 8-bit adder for signal <sum$addsub0070> created at line 64.

Found 8-bit adder for signal <sum$addsub0071> created at line 64.

Found 8-bit adder for signal <sum$addsub0072> created at line 64.

Found 8-bit adder for signal <sum$addsub0073> created at line 64.

Found 8-bit adder for signal <sum$addsub0074> created at line 64.

Found 8-bit adder for signal <sum$addsub0075> created at line 64.

Found 8-bit adder for signal <sum$addsub0076> created at line 64.

Found 8-bit adder for signal <sum$addsub0077> created at line 64.

Found 8-bit adder for signal <sum$addsub0078> created at line 64.

Found 8-bit adder for signal <sum$addsub0079> created at line 64.

Found 8-bit adder for signal <sum$addsub0080> created at line 64.

Found 8-bit adder for signal <sum$addsub0081> created at line 64.

Found 8-bit adder for signal <sum$addsub0082> created at line 64.

Found 8-bit adder for signal <sum$addsub0083> created at line 64.

Found 8-bit adder for signal <sum$addsub0084> created at line 64.

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Found 8-bit adder for signal <sum$addsub0086> created at line 64.

Found 8-bit adder for signal <sum$addsub0087> created at line 64.

Found 8-bit adder for signal <sum$addsub0088> created at line 64.

Found 8-bit adder for signal <sum$addsub0089> created at line 64.

Found 8-bit adder for signal <sum$addsub0090> created at line 64.

Found 8-bit adder for signal <sum$addsub0091> created at line 64.

Found 8-bit adder for signal <sum$addsub0092> created at line 64.

Found 8-bit adder for signal <sum$addsub0093> created at line 64.

Found 8-bit adder for signal <sum$addsub0094> created at line 64.

Found 8-bit adder for signal <sum$addsub0095> created at line 64.

Found 8-bit adder for signal <sum$addsub0096> created at line 64.

Found 8-bit adder for signal <sum$addsub0097> created at line 64.

Found 8-bit adder for signal <sum$addsub0098> created at line 64.

Found 8-bit adder for signal <sum$addsub0099> created at line 64.

Found 8-bit adder for signal <sum$addsub0100> created at line 64.

Found 8-bit adder for signal <sum$addsub0101> created at line 64.

Found 8-bit adder for signal <sum$addsub0102> created at line 64.

Found 8-bit adder for signal <sum$addsub0103> created at line 64.

Found 8-bit adder for signal <sum$addsub0104> created at line 64.

Found 8-bit adder for signal <sum$addsub0105> created at line 64.

Found 8-bit adder for signal <sum$addsub0106> created at line 64.

Found 8-bit adder for signal <sum$addsub0107> created at line 64.

Found 8-bit adder for signal <sum$addsub0108> created at line 64.

Found 8-bit adder for signal <sum$addsub0109> created at line 64.

Found 8-bit adder for signal <sum$addsub0110> created at line 64.

Found 8-bit adder for signal <sum$addsub0111> created at line 64.

Found 8-bit adder for signal <sum$addsub0112> created at line 64.

Found 8-bit adder for signal <sum$addsub0113> created at line 64.

Found 8-bit adder for signal <sum$addsub0114> created at line 64.

Found 8-bit adder for signal <sum$addsub0115> created at line 64.

Found 8-bit adder for signal <sum$addsub0116> created at line 64.

INFO:Xst:738 - HDL ADVISOR - 31775 flip-flops were inferred for signal <delayPipeline>. You may be trying to describe a RAM in a way that is incompatible with block and distributed RAM resources available on Xilinx devices, or with a specific template that is not supported. Please review the Xilinx resources documentation and the XST user manual for coding guidelines. Taking advantage of RAM resources will lead to improved device usage and reduced synthesis time.

Summary:

inferred 31783 D-type flip-flop(s).

inferred 135 Adder/Subtractor(s).

Unit <Houghtransform> synthesized.

Found 8-bit adder for signal <sum$addsub0085> created at line 64

=========================================================================

HDL Synthesis Report

Macro Statistics

# Adders/Subtractors : 135

8-bit adder : 135

# Registers : 31769

1-bit register : 31768

8-bit register : 1

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=========================================================================

\* Advanced HDL Synthesis \*

=========================================================================

=========================================================================

Advanced HDL Synthesis Report

Macro Statistics

# Adders/Subtractors : 134

8-bit adder : 133

8-bit adder carry in : 1

# Registers : 31776

Flip-Flops : 31776

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=========================================================================

\* Low Level Synthesis \*

=========================================================================

Optimizing unit <Houghtransform> ...

Mapping all equations...

Building and optimizing final netlist ...

Found area constraint ratio of 100 (+ 5) on block Houghtransform, actual ratio is 56.

Final Macro Processing ...

Processing Unit <Houghtransform> :

Found 9-bit shift register for signal <delayPipeline\_31767>.

Found 1008-bit shift register for signal <delayPipeline\_30744>.

Found 17-bit shift register for signal <delayPipeline\_30727>.

Found 1006-bit shift register for signal <delayPipeline\_29721>.

Found 19-bit shift register for signal <delayPipeline\_29702>.

Found 1004-bit shift register for signal <delayPipeline\_28698>.

Found 21-bit shift register for signal <delayPipeline\_28677>.

Found 1002-bit shift register for signal <delayPipeline\_27675>.

Found 23-bit shift register for signal <delayPipeline\_27652>.

Found 1000-bit shift register for signal <delayPipeline\_26652>.

Found 21-bit shift register for signal <delayPipeline\_26629>.

Found 998-bit shift register for signal <delayPipeline\_25629>.

Found 4-bit shift register for signal <delayPipeline\_25625>.

Found 19-bit shift register for signal <delayPipeline\_25606>.

Found 4-bit shift register for signal <delayPipeline\_25602>.

Found 996-bit shift register for signal <delayPipeline\_24606>.

Found 6-bit shift register for signal <delayPipeline\_24600>.

Found 17-bit shift register for signal <delayPipeline\_24583>.

Found 6-bit shift register for signal <delayPipeline\_24577>.

Found 994-bit shift register for signal <delayPipeline\_23583>.

Found 8-bit shift register for signal <delayPipeline\_23575>.

Found 15-bit shift register for signal <delayPipeline\_23560>.

Found 8-bit shift register for signal <delayPipeline\_23552>.

Found 993-bit shift register for signal <delayPipeline\_22559>.

Found 9-bit shift register for signal <delayPipeline\_22550>.

Found 13-bit shift register for signal <delayPipeline\_22537>.

Found 9-bit shift register for signal <delayPipeline\_22528>.

Found 993-bit shift register for signal <delayPipeline\_21535>.

Found 10-bit shift register for signal <delayPipeline\_21525>.

Found 11-bit shift register for signal <delayPipeline\_21514>.

Found 10-bit shift register for signal <delayPipeline\_21504>.

Found 993-bit shift register for signal <delayPipeline\_20511>.

Found 11-bit shift register for signal <delayPipeline\_20500>.

Found 9-bit shift register for signal <delayPipeline\_20491>.

Found 11-bit shift register for signal <delayPipeline\_20480>.

Found 993-bit shift register for signal <delayPipeline\_19487>.

Found 12-bit shift register for signal <delayPipeline\_19475>.

Found 7-bit shift register for signal <delayPipeline\_19468>.

Found 12-bit shift register for signal <delayPipeline\_19456>.

Found 993-bit shift register for signal <delayPipeline\_18463>.

Found 13-bit shift register for signal <delayPipeline\_18450>.

Found 5-bit shift register for signal <delayPipeline\_18445>.

Found 13-bit shift register for signal <delayPipeline\_18432>.

Found 993-bit shift register for signal <delayPipeline\_17439>.

Found 14-bit shift register for signal <delayPipeline\_17425>.

Found 14-bit shift register for signal <delayPipeline\_17408>.

Found 993-bit shift register for signal <delayPipeline\_16415>.

Found 15-bit shift register for signal <delayPipeline\_16400>.

Found 15-bit shift register for signal <delayPipeline\_16384>.

Found 993-bit shift register for signal <delayPipeline\_15391>.

Found 15-bit shift register for signal <delayPipeline\_15376>.

Found 15-bit shift register for signal <delayPipeline\_15360>.

Found 993-bit shift register for signal <delayPipeline\_14367>.

Found 14-bit shift register for signal <delayPipeline\_14353>.

Found 14-bit shift register for signal <delayPipeline\_14336>.

Found 993-bit shift register for signal <delayPipeline\_13343>.

Found 13-bit shift register for signal <delayPipeline\_13330>.

Found 5-bit shift register for signal <delayPipeline\_13325>.

Found 13-bit shift register for signal <delayPipeline\_13312>.

Found 993-bit shift register for signal <delayPipeline\_12319>.

Found 12-bit shift register for signal <delayPipeline\_12307>.

Found 7-bit shift register for signal <delayPipeline\_12300>.

Found 12-bit shift register for signal <delayPipeline\_12288>.

Found 993-bit shift register for signal <delayPipeline\_11295>.

Found 11-bit shift register for signal <delayPipeline\_11284>.

Found 9-bit shift register for signal <delayPipeline\_11275>.

Found 11-bit shift register for signal <delayPipeline\_11264>.

Found 993-bit shift register for signal <delayPipeline\_10271>.

Found 10-bit shift register for signal <delayPipeline\_10261>.

Found 11-bit shift register for signal <delayPipeline\_10250>.

Found 10-bit shift register for signal <delayPipeline\_10240>.

Found 993-bit shift register for signal <delayPipeline\_9247>.

Found 9-bit shift register for signal <delayPipeline\_9238>.

Found 13-bit shift register for signal <delayPipeline\_9225>.

Found 9-bit shift register for signal <delayPipeline\_9216>.

Found 993-bit shift register for signal <delayPipeline\_8223>.

Found 8-bit shift register for signal <delayPipeline\_8215>.

Found 15-bit shift register for signal <delayPipeline\_8200>.

Found 8-bit shift register for signal <delayPipeline\_8192>.

Found 994-bit shift register for signal <delayPipeline\_7198>.

Found 6-bit shift register for signal <delayPipeline\_7192>.

Found 17-bit shift register for signal <delayPipeline\_7175>.

Found 6-bit shift register for signal <delayPipeline\_7169>.

Found 996-bit shift register for signal <delayPipeline\_6173>.

Found 4-bit shift register for signal <delayPipeline\_6169>.

Found 19-bit shift register for signal <delayPipeline\_6150>.

Found 4-bit shift register for signal <delayPipeline\_6146>.

Found 998-bit shift register for signal <delayPipeline\_5148>.

Found 21-bit shift register for signal <delayPipeline\_5125>.

Found 1000-bit shift register for signal <delayPipeline\_4123>.

Found 23-bit shift register for signal <delayPipeline\_4100>.

Found 1002-bit shift register for signal <delayPipeline\_3098>.

Found 21-bit shift register for signal <delayPipeline\_3077>.

Found 1004-bit shift register for signal <delayPipeline\_2073>.

Found 19-bit shift register for signal <delayPipeline\_2054>.

Found 1006-bit shift register for signal <delayPipeline\_1048>.

Found 17-bit shift register for signal <delayPipeline\_1031>.

Found 1008-bit shift register for signal <delayPipeline\_23>.

Unit <Houghtransform> processed.

=========================================================================

Final Register Report

Macro Statistics

# Registers : 54

Flip-Flops : 54

# Shift Registers : 98

10-bit shift register : 4

1000-bit shift register : 2

1002-bit shift register : 2

1004-bit shift register : 2

1006-bit shift register : 2

1008-bit shift register : 2

11-bit shift register : 6

12-bit shift register : 4

13-bit shift register : 6

14-bit shift register : 4

15-bit shift register : 6

17-bit shift register : 4

19-bit shift register : 4

21-bit shift register : 4

23-bit shift register : 2

4-bit shift register : 4

5-bit shift register : 2

6-bit shift register : 4

7-bit shift register : 2

8-bit shift register : 4

9-bit shift register : 7

993-bit shift register : 15

994-bit shift register : 2

996-bit shift register : 2

998-bit shift register : 2

=========================================================================

=========================================================================

\* Partition Report \*

=========================================================================

Partition Implementation Status

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No Partitions were found in this design.

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=========================================================================

\* Final Report \*

=========================================================================

Clock Information:

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-----------------------------------+------------------------+-------+

Clock Signal | Clock buffer(FF name) | Load |

-----------------------------------+------------------------+-------+

clk | BUFGP | 2299 |

-----------------------------------+------------------------+-------+

Asynchronous Control Signals Information:

----------------------------------------

-----------------------------------+------------------------+-------+

Control Signal | Buffer(FF name) | Load |

-----------------------------------+------------------------+-------+

reset | BUFGP | 1159 |

-----------------------------------+------------------------+-------+

Timing Summary:

---------------

Speed Grade: -3

Minimum period: 12.530ns (Maximum Frequency: 79.812MHz)

Minimum input arrival time before clock: 1.338ns

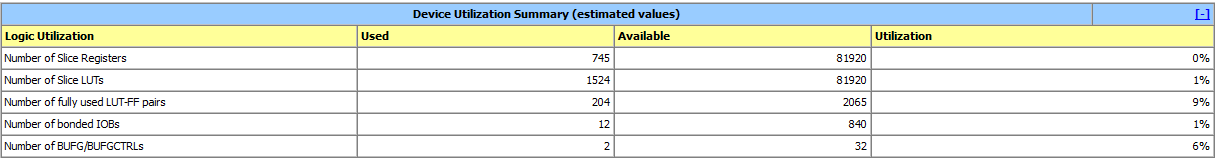
Maximum output required time after clock: 2.775ns

Maximum combinational path delay: No path found

=========================================================================

Process "Synthesize - XST" completed successfully

# 512x512, 32x32 Kreuz mit Kreis



Started : "Synthesize - XST".

Running xst...

Command Line: xst -intstyle ise -ifn "C:/Users/frank.schumacher/Merses/Work/VHDL/Correlation\_ShiftPipeline15052012/Houghtransform.xst" -ofn "C:/Users/frank.schumacher/Merses/Work/VHDL/Correlation\_ShiftPipeline15052012/Houghtransform.syr"

Reading design: Houghtransform.prj

=========================================================================

\* HDL Compilation \*

=========================================================================

Compiling vhdl file "C:/Users/frank.schumacher/Merses/Work/VHDL/Correlation\_ShiftPipeline15052012/source/imagedata.vhd" in Library work.

Package <testimage> compiled.

Compiling vhdl file "C:/Users/frank.schumacher/Merses/Work/VHDL/Correlation\_ShiftPipeline15052012/source/maskdata.vhd" in Library work.

Compiling vhdl file "C:/Users/frank.schumacher/Merses/Work/VHDL/Correlation\_ShiftPipeline15052012/source/referencedata.vhd" in Library work.

Package <referencedata> compiled.

Compiling vhdl file "C:/Users/frank.schumacher/Merses/Work/VHDL/Correlation\_ShiftPipeline15052012/source/topx0.vhd" in Library work.

Architecture behavioral of Entity houghtransform is up to date.

=========================================================================

\* Design Hierarchy Analysis \*

=========================================================================

Analyzing hierarchy for entity <Houghtransform> in library <work> (architecture <behavioral>).

=========================================================================

\* HDL Analysis \*

=========================================================================

Analyzing Entity <Houghtransform> in library <work> (Architecture <behavioral>).

Entity <Houghtransform> analyzed. Unit <Houghtransform> generated.

=========================================================================

\* HDL Synthesis \*

=========================================================================

Performing bidirectional port resolution...

Synthesizing Unit <Houghtransform>.

Related source file is "C:/Users/frank.schumacher/Merses/Work/VHDL/Correlation\_ShiftPipeline15052012/source/topx0.vhd".

WARNING:Xst:1780 - Signal <pixOut\_sig\_next> is never used or assigned. This unconnected signal will be trimmed during the optimization process.

WARNING:Xst:646 - Signal <delayPipeline<0><0>> is assigned but never used. This unconnected signal will be trimmed during the optimization process.

Found 8-bit register for signal <pixOut>.

Found 15903-bit register for signal <delayPipeline<1:15903>>.

Found 8-bit adder for signal <pixOut\_sig>.

Found 8-bit adder for signal <pixOut\_sig$addsub0000> created at line 64.

Found 8-bit adder for signal <pixOut\_sig$addsub0001> created at line 64.

Found 8-bit adder for signal <pixOut\_sig$addsub0002> created at line 64.

Found 8-bit adder for signal <pixOut\_sig$addsub0003> created at line 64.

Found 8-bit adder for signal <sum$add0000> created at line 64.

Found 8-bit adder for signal <sum$add0001> created at line 64.

Found 8-bit adder for signal <sum$add0002> created at line 64.

Found 8-bit adder for signal <sum$add0003> created at line 64.

Found 8-bit adder for signal <sum$add0004> created at line 64.

Found 8-bit adder for signal <sum$add0005> created at line 64.

Found 8-bit adder for signal <sum$add0006> created at line 64.

Found 8-bit adder for signal <sum$add0007> created at line 64.

Found 8-bit adder for signal <sum$add0008> created at line 64.

Found 8-bit adder for signal <sum$add0009> created at line 64.

Found 8-bit adder for signal <sum$add0010> created at line 64.

Found 8-bit adder for signal <sum$add0011> created at line 64.

Found 8-bit adder for signal <sum$add0012> created at line 64.

Found 8-bit adder for signal <sum$addsub0000> created at line 64.

Found 8-bit adder for signal <sum$addsub0001> created at line 64.

Found 8-bit adder for signal <sum$addsub0002> created at line 64.

Found 8-bit adder for signal <sum$addsub0003> created at line 64.

Found 8-bit adder for signal <sum$addsub0004> created at line 64.

Found 8-bit adder for signal <sum$addsub0005> created at line 64.

Found 8-bit adder for signal <sum$addsub0006> created at line 64.

Found 8-bit adder for signal <sum$addsub0007> created at line 64.

Found 8-bit adder for signal <sum$addsub0008> created at line 64.

Found 8-bit adder for signal <sum$addsub0009> created at line 64.

Found 8-bit adder for signal <sum$addsub0010> created at line 64.

Found 8-bit adder for signal <sum$addsub0011> created at line 64.

Found 8-bit adder for signal <sum$addsub0012> created at line 64.

Found 8-bit adder for signal <sum$addsub0013> created at line 64.

Found 8-bit adder for signal <sum$addsub0014> created at line 64.

Found 8-bit adder for signal <sum$addsub0015> created at line 64.

Found 8-bit adder for signal <sum$addsub0016> created at line 64.

Found 8-bit adder for signal <sum$addsub0017> created at line 64.

Found 8-bit adder for signal <sum$addsub0018> created at line 64.

Found 8-bit adder for signal <sum$addsub0019> created at line 64.

Found 8-bit adder for signal <sum$addsub0020> created at line 64.

Found 8-bit adder for signal <sum$addsub0021> created at line 64.

Found 8-bit adder for signal <sum$addsub0022> created at line 64.

Found 8-bit adder for signal <sum$addsub0023> created at line 64.

Found 8-bit adder for signal <sum$addsub0024> created at line 64.

Found 8-bit adder for signal <sum$addsub0025> created at line 64.

Found 8-bit adder for signal <sum$addsub0026> created at line 64.

Found 8-bit adder for signal <sum$addsub0027> created at line 64.

Found 8-bit adder for signal <sum$addsub0028> created at line 64.

Found 8-bit adder for signal <sum$addsub0029> created at line 64.

Found 8-bit adder for signal <sum$addsub0030> created at line 64.

Found 8-bit adder for signal <sum$addsub0031> created at line 64.

Found 8-bit adder for signal <sum$addsub0032> created at line 64.

Found 8-bit adder for signal <sum$addsub0033> created at line 64.

Found 8-bit adder for signal <sum$addsub0034> created at line 64.

Found 8-bit adder for signal <sum$addsub0035> created at line 64.

Found 8-bit adder for signal <sum$addsub0036> created at line 64.

Found 8-bit adder for signal <sum$addsub0037> created at line 64.

line 64.

Found 8-bit adder for signal <sum$addsub0039> created at line 64.

Found 8-bit adder for signal <sum$addsub0040> created at line 64.

Found 8-bit adder for signal <sum$addsub0041> created at line 64.

Found 8-bit adder for signal <sum$addsub0042> created at line 64.

Found 8-bit adder for signal <sum$addsub0043> created at line 64.

Found 8-bit adder for signal <sum$addsub0044> created at line 64.

Found 8-bit adder for signal <sum$addsub0045> created at line 64.

Found 8-bit adder for signal <sum$addsub0046> created at line 64.

Found 8-bit adder for signal <sum$addsub0047> created at line 64.

Found 8-bit adder for signal <sum$addsub0048> created at line 64.

Found 8-bit adder for signal <sum$addsub0049> created at line 64.

Found 8-bit adder for signal <sum$addsub0050> created at line 64.

Found 8-bit adder for signal <sum$addsub0051> created at line 64.

Found 8-bit adder for signal <sum$addsub0052> created at line 64.

Found 8-bit adder for signal <sum$addsub0053> created at line 64.

Found 8-bit adder for signal <sum$addsub0054> created at line 64.

Found 8-bit adder for signal <sum$addsub0055> created at line 64.

Found 8-bit adder for signal <sum$addsub0056> created at line 64.

Found 8-bit adder for signal <sum$addsub0057> created at line 64.

Found 8-bit adder for signal <sum$addsub0058> created at line 64.

Found 8-bit adder for signal <sum$addsub0059> created at line 64.

Found 8-bit adder for signal <sum$addsub0060> created at line 64.

Found 8-bit adder for signal <sum$addsub0061> created at line 64.

Found 8-bit adder for signal <sum$addsub0062> created at line 64.

Found 8-bit adder for signal <sum$addsub0063> created at line 64.

Found 8-bit adder for signal <sum$addsub0064> created at line 64.

Found 8-bit adder for signal <sum$addsub0065> created at line 64.

Found 8-bit adder for signal <sum$addsub0066> created at line 64.

Found 8-bit adder for signal <sum$addsub0067> created at line 64.

Found 8-bit adder for signal <sum$addsub0068> created at line 64.

Found 8-bit adder for signal <sum$addsub0069> created at line 64.

Found 8-bit adder for signal <sum$addsub0070> created at line 64.

Found 8-bit adder for signal <sum$addsub0071> created at line 64.

Found 8-bit adder for signal <sum$addsub0072> created at line 64.

Found 8-bit adder for signal <sum$addsub0073> created at line 64.

Found 8-bit adder for signal <sum$addsub0074> created at line 64.

Found 8-bit adder for signal <sum$addsub0075> created at line 64.

Found 8-bit adder for signal <sum$addsub0076> created at line 64.

Found 8-bit adder for signal <sum$addsub0077> created at line 64.

Found 8-bit adder for signal <sum$addsub0078> created at line 64.

Found 8-bit adder for signal <sum$addsub0079> created at line 64.

Found 8-bit adder for signal <sum$addsub0080> created at line 64.

Found 8-bit adder for signal <sum$addsub0081> created at line 64.

Found 8-bit adder for signal <sum$addsub0082> created at line 64.

Found 8-bit adder for signal <sum$addsub0083> created at line 64.

Found 8-bit adder for signal <sum$addsub0084> created at line 64.

Found 8-bit adder for signal <sum$addsub0085> created at line 64.

Found 8-bit adder for signal <sum$addsub0086> created at line 64.

Found 8-bit adder for signal <sum$addsub0087> created at line 64.

Found 8-bit adder for signal <sum$addsub0088> created at line 64.

Found 8-bit adder for signal <sum$addsub0089> created at line 64.

Found 8-bit adder for signal <sum$addsub0090> created at line 64.

Found 8-bit adder for signal <sum$addsub0091> created at line 64.

Found 8-bit adder for signal <sum$addsub0092> created at line 64.

Found 8-bit adder for signal <sum$addsub0038> created at Found 8-bit adder for signal <sum$addsub0093> created at line 64.

Found 8-bit adder for signal <sum$addsub0094> created at line 64.

Found 8-bit adder for signal <sum$addsub0095> created at line 64.

Found 8-bit adder for signal <sum$addsub0096> created at line 64.

Found 8-bit adder for signal <sum$addsub0097> created at line 64.

Found 8-bit adder for signal <sum$addsub0098> created at line 64.

Found 8-bit adder for signal <sum$addsub0099> created at line 64.

Found 8-bit adder for signal <sum$addsub0100> created at line 64.

Found 8-bit adder for signal <sum$addsub0101> created at line 64.

Found 8-bit adder for signal <sum$addsub0102> created at line 64.

Found 8-bit adder for signal <sum$addsub0103> created at line 64.

Found 8-bit adder for signal <sum$addsub0104> created at line 64.

Found 8-bit adder for signal <sum$addsub0105> created at line 64.

Found 8-bit adder for signal <sum$addsub0106> created at line 64.

Found 8-bit adder for signal <sum$addsub0107> created at line 64.

Found 8-bit adder for signal <sum$addsub0108> created at line 64.

Found 8-bit adder for signal <sum$addsub0109> created at line 64.

Found 8-bit adder for signal <sum$addsub0110> created at line 64.

Found 8-bit adder for signal <sum$addsub0111> created at line 64.

Found 8-bit adder for signal <sum$addsub0112> created at line 64.

Found 8-bit adder for signal <sum$addsub0113> created at line 64.

Found 8-bit adder for signal <sum$addsub0114> created at line 64.

Found 8-bit adder for signal <sum$addsub0115> created at line 64.

Found 8-bit adder for signal <sum$addsub0116> created at line 64.

INFO:Xst:738 - HDL ADVISOR - 15903 flip-flops were inferred for signal <delayPipeline>. You may be trying to describe a RAM in a way that is incompatible with block and distributed RAM resources available on Xilinx devices, or with a specific template that is not supported. Please review the Xilinx resources documentation and the XST user manual for coding guidelines. Taking advantage of RAM resources will lead to improved device usage and reduced synthesis time.

Summary:

inferred 15911 D-type flip-flop(s).

inferred 135 Adder/Subtractor(s).

Unit <Houghtransform> synthesized.

=========================================================================

HDL Synthesis Report

Macro Statistics

# Adders/Subtractors : 135

8-bit adder : 135

# Registers : 15897

1-bit register : 15896

8-bit register : 1

=========================================================================

=========================================================================

\* Advanced HDL Synthesis \*

=========================================================================

=========================================================================

Advanced HDL Synthesis Report

Macro Statistics

# Adders/Subtractors : 134

8-bit adder : 133

8-bit adder carry in : 1

# Registers : 15904

Flip-Flops : 15904

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=========================================================================

\* Low Level Synthesis \*

=========================================================================

Optimizing unit <Houghtransform> ...

Mapping all equations...

Building and optimizing final netlist ...

Found area constraint ratio of 100 (+ 5) on block Houghtransform, actual ratio is 28.

Final Macro Processing ...

Processing Unit <Houghtransform> :

Found 9-bit shift register for signal <delayPipeline\_15895>.

Found 496-bit shift register for signal <delayPipeline\_15384>.

Found 17-bit shift register for signal <delayPipeline\_15367>.

Found 494-bit shift register for signal <delayPipeline\_14873>.

Found 19-bit shift register for signal <delayPipeline\_14854>.

Found 492-bit shift register for signal <delayPipeline\_14362>.

Found 21-bit shift register for signal <delayPipeline\_14341>.

Found 490-bit shift register for signal <delayPipeline\_13851>.

Found 23-bit shift register for signal <delayPipeline\_13828>.

Found 488-bit shift register for signal <delayPipeline\_13340>.

Found 21-bit shift register for signal <delayPipeline\_13317>.

Found 486-bit shift register for signal <delayPipeline\_12829>.

Found 4-bit shift register for signal <delayPipeline\_12825>.

Found 19-bit shift register for signal <delayPipeline\_12806>.

Found 4-bit shift register for signal <delayPipeline\_12802>.

Found 484-bit shift register for signal <delayPipeline\_12318>.

Found 6-bit shift register for signal <delayPipeline\_12312>.

Found 17-bit shift register for signal <delayPipeline\_12295>.

Found 6-bit shift register for signal <delayPipeline\_12289>.

Found 482-bit shift register for signal <delayPipeline\_11807>.

Found 8-bit shift register for signal <delayPipeline\_11799>.

Found 15-bit shift register for signal <delayPipeline\_11784>.

Found 8-bit shift register for signal <delayPipeline\_11776>.

Found 481-bit shift register for signal <delayPipeline\_11295>.

Found 9-bit shift register for signal <delayPipeline\_11286>.

Found 13-bit shift register for signal <delayPipeline\_11273>.

Found 9-bit shift register for signal <delayPipeline\_11264>.

Found 481-bit shift register for signal <delayPipeline\_10783>.

Found 10-bit shift register for signal <delayPipeline\_10773>.

Found 11-bit shift register for signal <delayPipeline\_10762>.

Found 10-bit shift register for signal <delayPipeline\_10752>.

Found 481-bit shift register for signal <delayPipeline\_10271>.

Found 11-bit shift register for signal <delayPipeline\_10260>.

Found 9-bit shift register for signal <delayPipeline\_10251>.

Found 11-bit shift register for signal <delayPipeline\_10240>.

Found 481-bit shift register for signal <delayPipeline\_9759>.

Found 12-bit shift register for signal <delayPipeline\_9747>.

Found 7-bit shift register for signal <delayPipeline\_9740>.

Found 12-bit shift register for signal <delayPipeline\_9728>.

Found 481-bit shift register for signal <delayPipeline\_9247>.

Found 13-bit shift register for signal <delayPipeline\_9234>.

Found 5-bit shift register for signal <delayPipeline\_9229>.

Found 13-bit shift register for signal <delayPipeline\_9216>.

Found 481-bit shift register for signal <delayPipeline\_8735>.

Found 14-bit shift register for signal <delayPipeline\_8721>.

Found 14-bit shift register for signal <delayPipeline\_8704>.

Found 481-bit shift register for signal <delayPipeline\_8223>.

Found 15-bit shift register for signal <delayPipeline\_8208>.

Found 15-bit shift register for signal <delayPipeline\_8192>.

Found 481-bit shift register for signal <delayPipeline\_7711>.

Found 15-bit shift register for signal <delayPipeline\_7696>.

Found 15-bit shift register for signal <delayPipeline\_7680>.

Found 481-bit shift register for signal <delayPipeline\_7199>.

Found 14-bit shift register for signal <delayPipeline\_7185>.

Found 14-bit shift register for signal <delayPipeline\_7168>.

Found 481-bit shift register for signal <delayPipeline\_6687>.

Found 13-bit shift register for signal <delayPipeline\_6674>.

Found 5-bit shift register for signal <delayPipeline\_6669>.

Found 13-bit shift register for signal <delayPipeline\_6656>.

Found 481-bit shift register for signal <delayPipeline\_6175>.

Found 12-bit shift register for signal <delayPipeline\_6163>.

Found 7-bit shift register for signal <delayPipeline\_6156>.

Found 12-bit shift register for signal <delayPipeline\_6144>.

Found 481-bit shift register for signal <delayPipeline\_5663>.

Found 11-bit shift register for signal <delayPipeline\_5652>.

Found 9-bit shift register for signal <delayPipeline\_5643>.

Found 11-bit shift register for signal <delayPipeline\_5632>.

Found 481-bit shift register for signal <delayPipeline\_5151>.

Found 10-bit shift register for signal <delayPipeline\_5141>.

Found 11-bit shift register for signal <delayPipeline\_5130>.

Found 10-bit shift register for signal <delayPipeline\_5120>.

Found 481-bit shift register for signal <delayPipeline\_4639>.

Found 9-bit shift register for signal <delayPipeline\_4630>.

Found 13-bit shift register for signal <delayPipeline\_4617>.

Found 9-bit shift register for signal <delayPipeline\_4608>.

Found 481-bit shift register for signal <delayPipeline\_4127>.

Found 8-bit shift register for signal <delayPipeline\_4119>.

Found 15-bit shift register for signal <delayPipeline\_4104>.

Found 8-bit shift register for signal <delayPipeline\_4096>.

Found 482-bit shift register for signal <delayPipeline\_3614>.

Found 6-bit shift register for signal <delayPipeline\_3608>.

Found 17-bit shift register for signal <delayPipeline\_3591>.

Found 6-bit shift register for signal <delayPipeline\_3585>.

Found 484-bit shift register for signal <delayPipeline\_3101>.

Found 4-bit shift register for signal <delayPipeline\_3097>.

Found 19-bit shift register for signal <delayPipeline\_3078>.

Found 4-bit shift register for signal <delayPipeline\_3074>.

Found 486-bit shift register for signal <delayPipeline\_2588>.

Found 21-bit shift register for signal <delayPipeline\_2565>.

Found 488-bit shift register for signal <delayPipeline\_2075>.

Found 23-bit shift register for signal <delayPipeline\_2052>.

Found 490-bit shift register for signal <delayPipeline\_1562>.

Found 21-bit shift register for signal <delayPipeline\_1541>.

Found 492-bit shift register for signal <delayPipeline\_1049>.

Found 19-bit shift register for signal <delayPipeline\_1030>.

Found 494-bit shift register for signal <delayPipeline\_536>.

Found 17-bit shift register for signal <delayPipeline\_519>.

Found 496-bit shift register for signal <delayPipeline\_23>.

Unit <Houghtransform> processed.

=========================================================================

Final Register Report

Macro Statistics

# Registers : 54

Flip-Flops : 54

# Shift Registers : 98

10-bit shift register : 4

11-bit shift register : 6

12-bit shift register : 4

13-bit shift register : 6

14-bit shift register : 4

15-bit shift register : 6

17-bit shift register : 4

19-bit shift register : 4

21-bit shift register : 4

23-bit shift register : 2

4-bit shift register : 4

481-bit shift register : 15

482-bit shift register : 2

484-bit shift register : 2

486-bit shift register : 2

488-bit shift register : 2

490-bit shift register : 2

492-bit shift register : 2

494-bit shift register : 2

496-bit shift register : 2

5-bit shift register : 2

6-bit shift register : 4

7-bit shift register : 2

8-bit shift register : 4

9-bit shift register : 7

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\* Partition Report \*

=========================================================================

Partition Implementation Status

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No Partitions were found in this design.

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=========================================================================

\* Final Report \*

=========================================================================

Clock Information:

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-----------------------------------+------------------------+-------+

Clock Signal | Clock buffer(FF name) | Load |

-----------------------------------+------------------------+-------+

clk | BUFGP | 1291 |

-----------------------------------+------------------------+-------+

Asynchronous Control Signals Information:

----------------------------------------

-----------------------------------+------------------------+-------+

Control Signal | Buffer(FF name) | Load |

-----------------------------------+------------------------+-------+

reset | BUFGP | 647 |

-----------------------------------+------------------------+-------+

Timing Summary:

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Speed Grade: -3

Minimum period: 12.530ns (Maximum Frequency: **79.812MHz**)

Minimum input arrival time before clock: 1.338ns

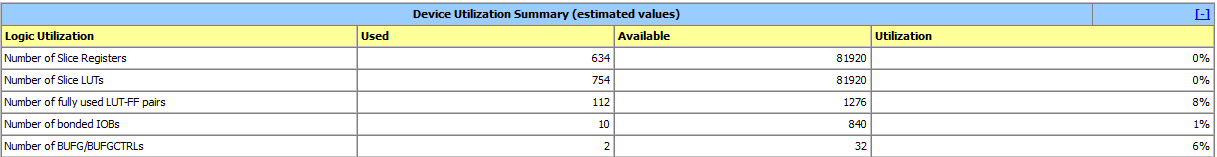
Maximum output required time after clock: 2.775ns

Maximum combinational path delay: No path found

=========================================================================

Process "Synthesize - XST" completed successfully

# 512x512, 29x11 Acht



Started : "Synthesize - XST".

Running xst...

Command Line: xst -intstyle ise -ifn "C:/Users/frank.schumacher/Merses/Work/VHDL/Correlation\_ShiftPipeline15052012/Houghtransform.xst" -ofn "C:/Users/frank.schumacher/Merses/Work/VHDL/Correlation\_ShiftPipeline15052012/Houghtransform.syr"

Reading design: Houghtransform.prj

=========================================================================

\* HDL Compilation \*

=========================================================================

Compiling vhdl file "C:/Users/frank.schumacher/Merses/Work/VHDL/Correlation\_ShiftPipeline15052012/source/imagedata.vhd" in Library work.

Package <testimage> compiled.

Compiling vhdl file "C:/Users/frank.schumacher/Merses/Work/VHDL/Correlation\_ShiftPipeline15052012/source/maskdata.vhd" in Library work.

Package <maskdata> compiled.

Compiling vhdl file "C:/Users/frank.schumacher/Merses/Work/VHDL/Correlation\_ShiftPipeline15052012/source/referencedata.vhd" in Library work.

Package <referencedata> compiled.

Compiling vhdl file "C:/Users/frank.schumacher/Merses/Work/VHDL/Correlation\_ShiftPipeline15052012/source/topx0.vhd" in Library work.

Architecture behavioral of Entity houghtransform is up to date.

=========================================================================

\* Design Hierarchy Analysis \*

=========================================================================

Analyzing hierarchy for entity <Houghtransform> in library <work> (architecture <behavioral>).

=========================================================================

\* HDL Analysis \*

=========================================================================

Analyzing Entity <Houghtransform> in library <work> (Architecture <behavioral>).

Entity <Houghtransform> analyzed. Unit <Houghtransform> generated.

=========================================================================

\* HDL Synthesis \*

=========================================================================

Performing bidirectional port resolution...

Synthesizing Unit <Houghtransform>.

Related source file is "C:/Users/frank.schumacher/Merses/Work/VHDL/Correlation\_ShiftPipeline15052012/source/topx0.vhd".

WARNING:Xst:1780 - Signal <pixOut\_sig\_next> is never used or assigned. This unconnected signal will be trimmed during the optimization process.

WARNING:Xst:646 - Signal <delayPipeline<0><0>> is assigned but never used. This unconnected signal will be trimmed during the optimization process.

Found 6-bit register for signal <pixOut>.

Found 14346-bit register for signal <delayPipeline<1:14346>>.

Found 6-bit adder for signal <pixOut\_sig>.

Found 6-bit adder for signal <pixOut\_sig$addsub0000> created at line 64.

Found 6-bit adder for signal <sum$add0000> created at line 64.

Found 6-bit adder for signal <sum$add0001> created at line 64.

Found 6-bit adder for signal <sum$add0002> created at line 64.

Found 6-bit adder for signal <sum$add0003> created at line 64.

Found 6-bit adder for signal <sum$add0004> created at line 64.

Found 6-bit adder for signal <sum$add0005> created at line 64.

Found 6-bit adder for signal <sum$addsub0000> created at line 64.

Found 6-bit adder for signal <sum$addsub0001> created at line 64.

Found 6-bit adder for signal <sum$addsub0002> created at line 64.

Found 6-bit adder for signal <sum$addsub0003> created at line 64.

Found 6-bit adder for signal <sum$addsub0004> created at line 64.

Found 6-bit adder for signal <sum$addsub0005> created at line 64.

Found 6-bit adder for signal <sum$addsub0006> created at line 64.

Found 6-bit adder for signal <sum$addsub0007> created at line 64.

Found 6-bit adder for signal <sum$addsub0008> created at line 64.

Found 6-bit adder for signal <sum$addsub0009> created at line 64.

Found 6-bit adder for signal <sum$addsub0010> created at line 64.

Found 6-bit adder for signal <sum$addsub0011> created at line 64.

Found 6-bit adder for signal <sum$addsub0012> created at line 64.

Found 6-bit adder for signal <sum$addsub0013> created at line 64.

Found 6-bit adder for signal <sum$addsub0014> created at line 64.

Found 6-bit adder for signal <sum$addsub0015> created at line 64.

Found 6-bit adder for signal <sum$addsub0016> created at line 64.

Found 6-bit adder for signal <sum$addsub0017> created at line 64.

Found 6-bit adder for signal <sum$addsub0018> created at line 64.

Found 6-bit adder for signal <sum$addsub0019> created at line 64.

Found 6-bit adder for signal <sum$addsub0021> created at line 64.

Found 6-bit adder for signal <sum$addsub0022> created at line 64.

Found 6-bit adder for signal <sum$addsub0023> created at line 64.

Found 6-bit adder for signal <sum$addsub0024> created at line 64.

Found 6-bit adder for signal <sum$addsub0025> created at line 64.

Found 6-bit adder for signal <sum$addsub0026> created at line 64.

Found 6-bit adder for signal <sum$addsub0027> created at line 64.

Found 6-bit adder for signal <sum$addsub0028> created at line 64.

Found 6-bit adder for signal <sum$addsub0029> created at line 64.

Found 6-bit adder for signal <sum$addsub0030> created at line 64.

Found 6-bit adder for signal <sum$addsub0031> created at line 64.

Found 6-bit adder for signal <sum$addsub0032> created at line 64.

Found 6-bit adder for signal <sum$addsub0033> created at line 64.

Found 6-bit adder for signal <sum$addsub0034> created at line 64.

Found 6-bit adder for signal <sum$addsub0035> created at line 64.

Found 6-bit adder for signal <sum$addsub0036> created at line 64.

Found 6-bit adder for signal <sum$addsub0037> created at line 64.

Found 6-bit adder for signal <sum$addsub0038> created at line 64.

Found 6-bit adder for signal <sum$addsub0039> created at line 64.

Found 6-bit adder for signal <sum$addsub0040> created at line 64.

Found 6-bit adder for signal <sum$addsub0041> created at line 64.

Found 6-bit adder for signal <sum$addsub0042> created at line 64.

Found 6-bit adder for signal <sum$addsub0043> created at line 64.

Found 6-bit adder for signal <sum$addsub0044> created at line 64.

Found 6-bit adder for signal <sum$addsub0045> created at line 64.

Found 6-bit adder for signal <sum$addsub0046> created at line 64.

Found 6-bit adder for signal <sum$addsub0047> created at line 64.

Found 6-bit adder for signal <sum$addsub0048> created at line 64.

Found 6-bit adder for signal <sum$addsub0049> created at line 64.

Found 6-bit adder for signal <sum$addsub0050> created at line 64.

Found 6-bit adder for signal <sum$addsub0051> created at line 64.

Found 6-bit adder for signal <sum$addsub0052> created at line 64.

Found 6-bit adder for signal <sum$addsub0053> created at line 64.

INFO:Xst:738 - HDL ADVISOR - 14346 flip-flops were inferred for signal <delayPipeline>. You may be trying to describe a RAM in a way that is incompatible with block and distributed RAM resources available on Xilinx devices, or with a specific template that is not supported. Please review the Xilinx resources documentation and the XST user manual for coding guidelines. Taking advantage of RAM resources will lead to improved device usage and reduced synthesis time.

Summary:

inferred 14352 D-type flip-flop(s).

inferred 62 Adder/Subtractor(s).

Unit <Houghtransform> synthesized.

Found 6-bit adder for signal <sum$addsub0020> created at line 64

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HDL Synthesis Report

Macro Statistics

# Adders/Subtractors : 62

6-bit adder : 62

# Registers : 14345

1-bit register : 14344

6-bit register : 1

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\* Advanced HDL Synthesis \*

=========================================================================

=========================================================================

Advanced HDL Synthesis Report

Macro Statistics

# Adders/Subtractors : 61

6-bit adder : 60

6-bit adder carry in : 1

# Registers : 14350

Flip-Flops : 14350

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\* Low Level Synthesis \*

=========================================================================

Optimizing unit <Houghtransform> ...

Mapping all equations...

Building and optimizing final netlist ...

Found area constraint ratio of 100 (+ 5) on block Houghtransform, actual ratio is 25.

Final Macro Processing ...

Processing Unit <Houghtransform> :

Found 4-bit shift register for signal <delayPipeline\_14343>.

Found 507-bit shift register for signal <delayPipeline\_13832>.

Found 6-bit shift register for signal <delayPipeline\_13826>.

Found 505-bit shift register for signal <delayPipeline\_13321>.

Found 8-bit shift register for signal <delayPipeline\_13313>.

Found 503-bit shift register for signal <delayPipeline\_12810>.

Found 10-bit shift register for signal <delayPipeline\_12800>.

Found 502-bit shift register for signal <delayPipeline\_12298>.

Found 10-bit shift register for signal <delayPipeline\_12288>.

Found 502-bit shift register for signal <delayPipeline\_11786>.

Found 10-bit shift register for signal <delayPipeline\_11776>.

Found 502-bit shift register for signal <delayPipeline\_11274>.

Found 10-bit shift register for signal <delayPipeline\_11264>.

Found 502-bit shift register for signal <delayPipeline\_10762>.

Found 10-bit shift register for signal <delayPipeline\_10752>.

Found 502-bit shift register for signal <delayPipeline\_10250>.

Found 10-bit shift register for signal <delayPipeline\_10240>.

Found 502-bit shift register for signal <delayPipeline\_9738>.

Found 10-bit shift register for signal <delayPipeline\_9728>.

Found 503-bit shift register for signal <delayPipeline\_9225>.

Found 8-bit shift register for signal <delayPipeline\_9217>.

Found 505-bit shift register for signal <delayPipeline\_8712>.

Found 6-bit shift register for signal <delayPipeline\_8706>.

Found 507-bit shift register for signal <delayPipeline\_8199>.

Found 4-bit shift register for signal <delayPipeline\_8195>.

Found 509-bit shift register for signal <delayPipeline\_7686>.

Found 511-bit shift register for signal <delayPipeline\_7173>.

Found 511-bit shift register for signal <delayPipeline\_6662>.

Found 509-bit shift register for signal <delayPipeline\_6151>.

Found 4-bit shift register for signal <delayPipeline\_6147>.

Found 507-bit shift register for signal <delayPipeline\_5640>.

Found 6-bit shift register for signal <delayPipeline\_5634>.

Found 505-bit shift register for signal <delayPipeline\_5129>.

Found 8-bit shift register for signal <delayPipeline\_5121>.

Found 503-bit shift register for signal <delayPipeline\_4618>.

Found 10-bit shift register for signal <delayPipeline\_4608>.

Found 502-bit shift register for signal <delayPipeline\_4106>.

Found 10-bit shift register for signal <delayPipeline\_4096>.

Found 502-bit shift register for signal <delayPipeline\_3594>.

Found 10-bit shift register for signal <delayPipeline\_3584>.

Found 502-bit shift register for signal <delayPipeline\_3082>.

Found 10-bit shift register for signal <delayPipeline\_3072>.

Found 502-bit shift register for signal <delayPipeline\_2570>.

Found 10-bit shift register for signal <delayPipeline\_2560>.

Found 502-bit shift register for signal <delayPipeline\_2058>.

Found 10-bit shift register for signal <delayPipeline\_2048>.

Found 502-bit shift register for signal <delayPipeline\_1546>.

Found 10-bit shift register for signal <delayPipeline\_1536>.

Found 503-bit shift register for signal <delayPipeline\_1033>.

Found 8-bit shift register for signal <delayPipeline\_1025>.

Found 505-bit shift register for signal <delayPipeline\_520>.

Found 6-bit shift register for signal <delayPipeline\_514>.

Found 507-bit shift register for signal <delayPipeline\_7>.

Unit <Houghtransform> processed.

=========================================================================

Final Register Report

Macro Statistics

# Registers : 18

Flip-Flops : 18

# Shift Registers : 53

10-bit shift register : 14

4-bit shift register : 3

502-bit shift register : 12

503-bit shift register : 4

505-bit shift register : 4

507-bit shift register : 4

509-bit shift register : 2

511-bit shift register : 2

6-bit shift register : 4

8-bit shift register : 4

=========================================================================

=========================================================================

\* Partition Report \*

=========================================================================

Partition Implementation Status

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No Partitions were found in this design.

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=========================================================================

\* Final Report \*

=========================================================================

Clock Information:

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-----------------------------------+------------------------+-------+

Clock Signal | Clock buffer(FF name) | Load |

-----------------------------------+------------------------+-------+

clk | BUFGP | 1107 |

-----------------------------------+------------------------+-------+

Asynchronous Control Signals Information:

----------------------------------------

-----------------------------------+------------------------+-------+

Control Signal | Buffer(FF name) | Load |

-----------------------------------+------------------------+-------+

reset | BUFGP | 581 |

-----------------------------------+------------------------+-------+

Timing Summary:

---------------

Speed Grade: -3

Minimum period: 8.381ns (Maximum Frequency: **119.322MHz**)

Minimum input arrival time before clock: 1.338ns

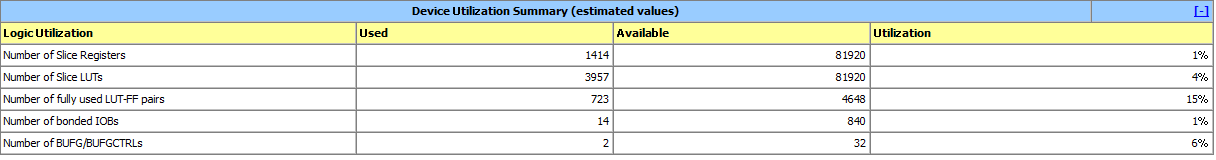
Maximum output required time after clock: 2.775ns

Maximum combinational path delay: No path found

=========================================================================

Process "Synthesize - XST" completed successfully

# 512x512, 64x64 Template



Started : "Synthesize - XST".

Running xst...

Command Line: xst -intstyle ise -ifn "C:/Users/frank.schumacher/Merses/Work/VHDL/Correlation\_ShiftPipeline15052012/Houghtransform.xst" -ofn "C:/Users/frank.schumacher/Merses/Work/VHDL/Correlation\_ShiftPipeline15052012/Houghtransform.syr"

Reading design: Houghtransform.prj

=========================================================================

\* HDL Compilation \*

=========================================================================

Compiling vhdl file "C:/Users/frank.schumacher/Merses/Work/VHDL/Correlation\_ShiftPipeline15052012/source/imagedata.vhd" in Library work.

Compiling vhdl file "C:/Users/frank.schumacher/Merses/Work/VHDL/Correlation\_ShiftPipeline15052012/source/maskdata.vhd" in Library work.

Compiling vhdl file "C:/Users/frank.schumacher/Merses/Work/VHDL/Correlation\_ShiftPipeline15052012/source/referencedata.vhd" in Library work.

Compiling vhdl file "C:/Users/frank.schumacher/Merses/Work/VHDL/Correlation\_ShiftPipeline15052012/source/topx0.vhd" in Library work.

Architecture behavioral of Entity houghtransform is up to date.

=========================================================================

\* Design Hierarchy Analysis \*

=========================================================================

Analyzing hierarchy for entity <Houghtransform> in library <work> (architecture <behavioral>).

=========================================================================

\* HDL Analysis \*

=========================================================================

Analyzing Entity <Houghtransform> in library <work> (Architecture <behavioral>).

Entity <Houghtransform> analyzed. Unit <Houghtransform> generated.

=========================================================================

\* HDL Synthesis \*

=========================================================================

Performing bidirectional port resolution...

Synthesizing Unit <Houghtransform>.

Related source file is "C:/Users/frank.schumacher/Merses/Work/VHDL/Correlation\_ShiftPipeline15052012/source/topx0.vhd".

WARNING:Xst:1780 - Signal <pixOut\_sig\_next> is never used or assigned. This unconnected signal will be trimmed during the optimization process.

WARNING:Xst:646 - Signal <delayPipeline<0><0>> is assigned but never used. This unconnected signal will be trimmed during the optimization process.

Found 10-bit register for signal <pixOut>.

Found 32319-bit register for signal <delayPipeline<1:32319>>.

Found 10-bit adder for signal <pixOut\_sig>.

Found 10-bit adder for signal <pixOut\_sig$addsub0000> created at line 64.

Found 10-bit adder for signal <pixOut\_sig$addsub0001> created at line 64.

Found 10-bit adder for signal <sum$add0000> created at line 64.

Found 10-bit adder for signal <sum$add0001> created at line 64.

Found 10-bit adder for signal <sum$add0002> created at line 64.

Found 10-bit adder for signal <sum$add0003> created at line 64.

Found 10-bit adder for signal <sum$add0004> created at line 64.

Found 10-bit adder for signal <sum$add0005> created at line 64.

Found 10-bit adder for signal <sum$add0006> created at line 64.

Found 10-bit adder for signal <sum$add0007> created at line 64.

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Found 10-bit adder for signal <sum$add0010> created at line 64.

Found 10-bit adder for signal <sum$add0011> created at line 64.

Found 10-bit adder for signal <sum$add0012> created at line 64.

Found 10-bit adder for signal <sum$add0013> created at line 64.

Found 10-bit adder for signal <sum$add0014> created at line 64.

Found 10-bit adder for signal <sum$add0015> created at line 64.

Found 10-bit adder for signal <sum$add0016> created at line 64.

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Found 10-bit adder for signal <sum$add0019> created at line 64.

Found 10-bit adder for signal <sum$add0020> created at line 64.

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Found 10-bit adder for signal <sum$add0030> created at line 64.

Found 10-bit adder for signal <sum$add0031> created at line 64.

Found 10-bit adder for signal <sum$add0032> created at line 64.

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Found 10-bit adder for signal <sum$add0042> created at line 64.

Found 10-bit adder for signal <sum$add0043> created at line 64.

Found 10-bit adder for signal <sum$add0044> created at line 64.

Found 10-bit adder for signal <sum$add0045> created at line 64.

Found 10-bit adder for signal <sum$add0046> created at line 64.

Found 10-bit adder for signal <sum$add0047> created at line 64.

Found 10-bit adder for signal <sum$add0048> created at line 64.

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Found 10-bit adder for signal <sum$add0050> created at line 64.

Found 10-bit adder for signal <sum$add0051> created at line 64.

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Found 10-bit adder for signal <sum$addsub0000> created at line 64.

Found 10-bit adder for signal <sum$addsub0001> created at line 64.

Found 10-bit adder for signal <sum$addsub0002> created at line 64.

Found 10-bit adder for signal <sum$addsub0003> created at line 64.

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Found 10-bit adder for signal <sum$addsub0012> created at line 64.

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Found 10-bit adder for signal <sum$addsub0014> created at line 64.

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Found 10-bit adder for signal <sum$addsub0111> created at line 64.

Found 10-bit adder for signal <sum$addsub0112> created at line 64.

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Found 10-bit adder for signal <sum$addsub0200> created at line 64.

Found 10-bit adder for signal <sum$addsub0201> created at line 64.

Found 10-bit adder for signal <sum$addsub0202> created at line 64.

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Found 10-bit adder for signal <sum$addsub0234> created at line 64.

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Found 10-bit adder for signal <sum$addsub0250> created at line 64.

Found 10-bit adder for signal <sum$addsub0251> created at line 64.

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Found 10-bit adder for signal <sum$addsub0264> created at line 64.

Found 10-bit adder for signal <sum$addsub0265> created at line 64.

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Found 10-bit adder for signal <sum$addsub0450> created at line 64.

Found 10-bit adder for signal <sum$addsub0451> created at line 64.

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Found 10-bit adder for signal <sum$addsub0464> created at line 64.

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Found 10-bit adder for signal <sum$addsub0482> created at line 64.

Found 10-bit adder for signal <sum$addsub0483> created at line 64.

Found 10-bit adder for signal <sum$addsub0484> created at line 64.

Found 10-bit adder for signal <sum$addsub0485> created at line 64.

INFO:Xst:738 - HDL ADVISOR - 32319 flip-flops were inferred for signal <delayPipeline>. You may be trying to describe a RAM in a way that is incompatible with block and distributed RAM resources available on Xilinx devices, or with a specific template that is not supported. Please review the Xilinx resources documentation and the XST user manual for coding guidelines. Taking advantage of RAM resources will lead to improved device usage and reduced synthesis time.

Summary:

inferred 32329 D-type flip-flop(s).

inferred 543 Adder/Subtractor(s).

Unit <Houghtransform> synthesized.

=========================================================================

HDL Synthesis Report

Macro Statistics

# Adders/Subtractors : 543

10-bit adder : 543

# Registers : 32313

1-bit register : 32312

10-bit register : 1

=========================================================================

=========================================================================

\* Advanced HDL Synthesis \*

=========================================================================

=========================================================================

Advanced HDL Synthesis Report

Macro Statistics

# Adders/Subtractors : 542

10-bit adder : 541

10-bit adder carry in : 1

# Registers : 32322

Flip-Flops : 32322

=========================================================================

=========================================================================

\* Low Level Synthesis \*

=========================================================================

Optimizing unit <Houghtransform> ...

Mapping all equations...

Building and optimizing final netlist ...

Found area constraint ratio of 100 (+ 5) on block Houghtransform, actual ratio is 61.

Final Macro Processing ...

Processing Unit <Houghtransform> :

Found 9-bit shift register for signal <delayPipeline\_32311>.

Found 17-bit shift register for signal <delayPipeline\_32279>.

Found 464-bit shift register for signal <delayPipeline\_31800>.

Found 17-bit shift register for signal <delayPipeline\_31783>.

Found 15-bit shift register for signal <delayPipeline\_31768>.

Found 17-bit shift register for signal <delayPipeline\_31751>.

Found 462-bit shift register for signal <delayPipeline\_31289>.

Found 19-bit shift register for signal <delayPipeline\_31270>.

Found 13-bit shift register for signal <delayPipeline\_31257>.

Found 19-bit shift register for signal <delayPipeline\_31238>.

Found 460-bit shift register for signal <delayPipeline\_30778>.

Found 21-bit shift register for signal <delayPipeline\_30757>.

Found 11-bit shift register for signal <delayPipeline\_30746>.

Found 21-bit shift register for signal <delayPipeline\_30725>.

Found 458-bit shift register for signal <delayPipeline\_30267>.

Found 23-bit shift register for signal <delayPipeline\_30244>.

Found 9-bit shift register for signal <delayPipeline\_30235>.

Found 23-bit shift register for signal <delayPipeline\_30212>.

Found 456-bit shift register for signal <delayPipeline\_29756>.

Found 21-bit shift register for signal <delayPipeline\_29733>.

Found 7-bit shift register for signal <delayPipeline\_29724>.

Found 21-bit shift register for signal <delayPipeline\_29701>.

Found 454-bit shift register for signal <delayPipeline\_29245>.

Found 4-bit shift register for signal <delayPipeline\_29241>.

Found 19-bit shift register for signal <delayPipeline\_29222>.

Found 4-bit shift register for signal <delayPipeline\_29218>.

Found 5-bit shift register for signal <delayPipeline\_29213>.

Found 4-bit shift register for signal <delayPipeline\_29209>.

Found 19-bit shift register for signal <delayPipeline\_29190>.

Found 4-bit shift register for signal <delayPipeline\_29186>.

Found 452-bit shift register for signal <delayPipeline\_28734>.

Found 6-bit shift register for signal <delayPipeline\_28728>.

Found 17-bit shift register for signal <delayPipeline\_28711>.

Found 6-bit shift register for signal <delayPipeline\_28705>.

Found 6-bit shift register for signal <delayPipeline\_28696>.

Found 17-bit shift register for signal <delayPipeline\_28679>.

Found 6-bit shift register for signal <delayPipeline\_28673>.

Found 450-bit shift register for signal <delayPipeline\_28223>.

Found 8-bit shift register for signal <delayPipeline\_28215>.

Found 15-bit shift register for signal <delayPipeline\_28200>.

Found 8-bit shift register for signal <delayPipeline\_28192>.

Found 8-bit shift register for signal <delayPipeline\_28183>.

Found 15-bit shift register for signal <delayPipeline\_28168>.

Found 8-bit shift register for signal <delayPipeline\_28160>.

Found 449-bit shift register for signal <delayPipeline\_27711>.

Found 9-bit shift register for signal <delayPipeline\_27702>.

Found 13-bit shift register for signal <delayPipeline\_27689>.

Found 9-bit shift register for signal <delayPipeline\_27680>.

Found 9-bit shift register for signal <delayPipeline\_27670>.

Found 13-bit shift register for signal <delayPipeline\_27657>.

Found 9-bit shift register for signal <delayPipeline\_27648>.

Found 449-bit shift register for signal <delayPipeline\_27199>.

Found 10-bit shift register for signal <delayPipeline\_27189>.

Found 11-bit shift register for signal <delayPipeline\_27178>.

Found 10-bit shift register for signal <delayPipeline\_27168>.

Found 10-bit shift register for signal <delayPipeline\_27157>.

Found 11-bit shift register for signal <delayPipeline\_27146>.

Found 10-bit shift register for signal <delayPipeline\_27136>.

Found 449-bit shift register for signal <delayPipeline\_26687>.

Found 11-bit shift register for signal <delayPipeline\_26676>.

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Found 11-bit shift register for signal <delayPipeline\_26656>.

Found 11-bit shift register for signal <delayPipeline\_26644>.

Found 9-bit shift register for signal <delayPipeline\_26635>.

Found 11-bit shift register for signal <delayPipeline\_26624>.

Found 449-bit shift register for signal <delayPipeline\_26175>.

Found 12-bit shift register for signal <delayPipeline\_26163>.

Found 7-bit shift register for signal <delayPipeline\_26156>.

Found 12-bit shift register for signal <delayPipeline\_26144>.

Found 12-bit shift register for signal <delayPipeline\_26131>.

Found 7-bit shift register for signal <delayPipeline\_26124>.

Found 12-bit shift register for signal <delayPipeline\_26112>.

Found 449-bit shift register for signal <delayPipeline\_25663>.

Found 13-bit shift register for signal <delayPipeline\_25650>.

Found 5-bit shift register for signal <delayPipeline\_25645>.

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Found 13-bit shift register for signal <delayPipeline\_25618>.

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Found 13-bit shift register for signal <delayPipeline\_25600>.

Found 449-bit shift register for signal <delayPipeline\_25151>.

Found 14-bit shift register for signal <delayPipeline\_25137>.

Found 14-bit shift register for signal <delayPipeline\_25120>.

Found 14-bit shift register for signal <delayPipeline\_25105>.

Found 14-bit shift register for signal <delayPipeline\_25088>.

Found 449-bit shift register for signal <delayPipeline\_24639>.

Found 15-bit shift register for signal <delayPipeline\_24624>.

Found 15-bit shift register for signal <delayPipeline\_24608>.

Found 15-bit shift register for signal <delayPipeline\_24592>.

Found 15-bit shift register for signal <delayPipeline\_24576>.

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Found 15-bit shift register for signal <delayPipeline\_24112>.

Found 15-bit shift register for signal <delayPipeline\_24096>.

Found 15-bit shift register for signal <delayPipeline\_24080>.

Found 15-bit shift register for signal <delayPipeline\_24064>.

Found 449-bit shift register for signal <delayPipeline\_23615>.

Found 14-bit shift register for signal <delayPipeline\_23601>.

Found 14-bit shift register for signal <delayPipeline\_23584>.

Found 14-bit shift register for signal <delayPipeline\_23569>.

Found 14-bit shift register for signal <delayPipeline\_23552>.

Found 449-bit shift register for signal <delayPipeline\_23103>.

Found 13-bit shift register for signal <delayPipeline\_23090>.

Found 5-bit shift register for signal <delayPipeline\_23085>.

Found 13-bit shift register for signal <delayPipeline\_23072>.

Found 13-bit shift register for signal <delayPipeline\_23058>.

Found 5-bit shift register for signal <delayPipeline\_23053>.

Found 13-bit shift register for signal <delayPipeline\_23040>.

Found 449-bit shift register for signal <delayPipeline\_22591>.

Found 12-bit shift register for signal <delayPipeline\_22579>.

Found 7-bit shift register for signal <delayPipeline\_22572>.

Found 12-bit shift register for signal <delayPipeline\_22560>.

Found 12-bit shift register for signal <delayPipeline\_22547>.

Found 7-bit shift register for signal <delayPipeline\_22540>.

Found 12-bit shift register for signal <delayPipeline\_22528>.

Found 449-bit shift register for signal <delayPipeline\_22079>.

Found 11-bit shift register for signal <delayPipeline\_22068>.

Found 9-bit shift register for signal <delayPipeline\_22059>.

Found 11-bit shift register for signal <delayPipeline\_22048>.

Found 11-bit shift register for signal <delayPipeline\_22036>.

Found 9-bit shift register for signal <delayPipeline\_22027>.

Found 11-bit shift register for signal <delayPipeline\_22016>.

Found 449-bit shift register for signal <delayPipeline\_21567>.

Found 10-bit shift register for signal <delayPipeline\_21557>.

Found 11-bit shift register for signal <delayPipeline\_21546>.

Found 10-bit shift register for signal <delayPipeline\_21536>.

Found 10-bit shift register for signal <delayPipeline\_21525>.

Found 11-bit shift register for signal <delayPipeline\_21514>.

Found 10-bit shift register for signal <delayPipeline\_21504>.

Found 449-bit shift register for signal <delayPipeline\_21055>.

Found 9-bit shift register for signal <delayPipeline\_21046>.

Found 13-bit shift register for signal <delayPipeline\_21033>.

Found 9-bit shift register for signal <delayPipeline\_21024>.

Found 9-bit shift register for signal <delayPipeline\_21014>.

Found 13-bit shift register for signal <delayPipeline\_21001>.

Found 9-bit shift register for signal <delayPipeline\_20992>.

Found 449-bit shift register for signal <delayPipeline\_20543>.

Found 8-bit shift register for signal <delayPipeline\_20535>.

Found 15-bit shift register for signal <delayPipeline\_20520>.

Found 8-bit shift register for signal <delayPipeline\_20512>.

Found 8-bit shift register for signal <delayPipeline\_20503>.

Found 15-bit shift register for signal <delayPipeline\_20488>.

Found 8-bit shift register for signal <delayPipeline\_20480>.

Found 450-bit shift register for signal <delayPipeline\_20030>.

Found 6-bit shift register for signal <delayPipeline\_20024>.

Found 17-bit shift register for signal <delayPipeline\_20007>.

Found 6-bit shift register for signal <delayPipeline\_20001>.

Found 6-bit shift register for signal <delayPipeline\_19992>.

Found 17-bit shift register for signal <delayPipeline\_19975>.

Found 6-bit shift register for signal <delayPipeline\_19969>.

Found 452-bit shift register for signal <delayPipeline\_19517>.

Found 4-bit shift register for signal <delayPipeline\_19513>.

Found 19-bit shift register for signal <delayPipeline\_19494>.

Found 4-bit shift register for signal <delayPipeline\_19490>.

Found 5-bit shift register for signal <delayPipeline\_19485>.

Found 4-bit shift register for signal <delayPipeline\_19481>.

Found 19-bit shift register for signal <delayPipeline\_19462>.

Found 4-bit shift register for signal <delayPipeline\_19458>.

Found 454-bit shift register for signal <delayPipeline\_19004>.

Found 21-bit shift register for signal <delayPipeline\_18981>.

Found 7-bit shift register for signal <delayPipeline\_18972>.

Found 21-bit shift register for signal <delayPipeline\_18949>.

Found 456-bit shift register for signal <delayPipeline\_18491>.

Found 23-bit shift register for signal <delayPipeline\_18468>.

Found 9-bit shift register for signal <delayPipeline\_18459>.

Found 23-bit shift register for signal <delayPipeline\_18436>.

Found 458-bit shift register for signal <delayPipeline\_17978>.

Found 21-bit shift register for signal <delayPipeline\_17957>.

Found 11-bit shift register for signal <delayPipeline\_17946>.

Found 21-bit shift register for signal <delayPipeline\_17925>.

Found 460-bit shift register for signal <delayPipeline\_17465>.

Found 19-bit shift register for signal <delayPipeline\_17446>.

Found 13-bit shift register for signal <delayPipeline\_17433>.

Found 19-bit shift register for signal <delayPipeline\_17414>.

Found 462-bit shift register for signal <delayPipeline\_16952>.

Found 17-bit shift register for signal <delayPipeline\_16935>.

Found 15-bit shift register for signal <delayPipeline\_16920>.

Found 17-bit shift register for signal <delayPipeline\_16903>.

Found 464-bit shift register for signal <delayPipeline\_16439>.

Found 17-bit shift register for signal <delayPipeline\_16407>.

Found 465-bit shift register for signal <delayPipeline\_15927>.

Found 17-bit shift register for signal <delayPipeline\_15895>.

Found 464-bit shift register for signal <delayPipeline\_15416>.

Found 17-bit shift register for signal <delayPipeline\_15399>.

Found 15-bit shift register for signal <delayPipeline\_15384>.

Found 17-bit shift register for signal <delayPipeline\_15367>.

Found 462-bit shift register for signal <delayPipeline\_14905>.

Found 19-bit shift register for signal <delayPipeline\_14886>.

Found 13-bit shift register for signal <delayPipeline\_14873>.

Found 19-bit shift register for signal <delayPipeline\_14854>.

Found 460-bit shift register for signal <delayPipeline\_14394>.

Found 21-bit shift register for signal <delayPipeline\_14373>.

Found 11-bit shift register for signal <delayPipeline\_14362>.

Found 21-bit shift register for signal <delayPipeline\_14341>.

Found 458-bit shift register for signal <delayPipeline\_13883>.

Found 23-bit shift register for signal <delayPipeline\_13860>.

Found 9-bit shift register for signal <delayPipeline\_13851>.

Found 23-bit shift register for signal <delayPipeline\_13828>.

Found 456-bit shift register for signal <delayPipeline\_13372>.

Found 21-bit shift register for signal <delayPipeline\_13349>.

Found 7-bit shift register for signal <delayPipeline\_13340>.

Found 21-bit shift register for signal <delayPipeline\_13317>.

Found 454-bit shift register for signal <delayPipeline\_12861>.

Found 4-bit shift register for signal <delayPipeline\_12857>.

Found 19-bit shift register for signal <delayPipeline\_12838>.

Found 4-bit shift register for signal <delayPipeline\_12834>.

Found 5-bit shift register for signal <delayPipeline\_12829>.

Found 4-bit shift register for signal <delayPipeline\_12825>.

Found 19-bit shift register for signal <delayPipeline\_12806>.

Found 4-bit shift register for signal <delayPipeline\_12802>.

Found 452-bit shift register for signal <delayPipeline\_12350>.

Found 6-bit shift register for signal <delayPipeline\_12344>.

Found 17-bit shift register for signal <delayPipeline\_12327>.

Found 6-bit shift register for signal <delayPipeline\_12321>.

Found 6-bit shift register for signal <delayPipeline\_12312>.

Found 17-bit shift register for signal <delayPipeline\_12295>.

Found 6-bit shift register for signal <delayPipeline\_12289>.

Found 450-bit shift register for signal <delayPipeline\_11839>.

Found 8-bit shift register for signal <delayPipeline\_11831>.

Found 15-bit shift register for signal <delayPipeline\_11816>.

Found 8-bit shift register for signal <delayPipeline\_11808>.

Found 8-bit shift register for signal <delayPipeline\_11799>.

Found 15-bit shift register for signal <delayPipeline\_11784>.

Found 8-bit shift register for signal <delayPipeline\_11776>.

Found 449-bit shift register for signal <delayPipeline\_11327>.

Found 9-bit shift register for signal <delayPipeline\_11318>.

Found 13-bit shift register for signal <delayPipeline\_11305>.

Found 9-bit shift register for signal <delayPipeline\_11296>.

Found 9-bit shift register for signal <delayPipeline\_11286>.

Found 13-bit shift register for signal <delayPipeline\_11273>.

Found 9-bit shift register for signal <delayPipeline\_11264>.

Found 449-bit shift register for signal <delayPipeline\_10815>.

Found 10-bit shift register for signal <delayPipeline\_10805>.

Found 11-bit shift register for signal <delayPipeline\_10794>.

Found 10-bit shift register for signal <delayPipeline\_10784>.

Found 10-bit shift register for signal <delayPipeline\_10773>.

Found 11-bit shift register for signal <delayPipeline\_10762>.

Found 10-bit shift register for signal <delayPipeline\_10752>.

Found 449-bit shift register for signal <delayPipeline\_10303>.

Found 11-bit shift register for signal <delayPipeline\_10292>.

Found 9-bit shift register for signal <delayPipeline\_10283>.

Found 11-bit shift register for signal <delayPipeline\_10272>.

Found 11-bit shift register for signal <delayPipeline\_10260>.

Found 9-bit shift register for signal <delayPipeline\_10251>.

Found 11-bit shift register for signal <delayPipeline\_10240>.

Found 449-bit shift register for signal <delayPipeline\_9791>.

Found 12-bit shift register for signal <delayPipeline\_9779>.

Found 7-bit shift register for signal <delayPipeline\_9772>.

Found 12-bit shift register for signal <delayPipeline\_9760>.

Found 12-bit shift register for signal <delayPipeline\_9747>.

Found 7-bit shift register for signal <delayPipeline\_9740>.

Found 12-bit shift register for signal <delayPipeline\_9728>.

Found 449-bit shift register for signal <delayPipeline\_9279>.

Found 13-bit shift register for signal <delayPipeline\_9266>.

Found 5-bit shift register for signal <delayPipeline\_9261>.

Found 13-bit shift register for signal <delayPipeline\_9248>.

Found 13-bit shift register for signal <delayPipeline\_9234>.

Found 5-bit shift register for signal <delayPipeline\_9229>.

Found 13-bit shift register for signal <delayPipeline\_9216>.

Found 449-bit shift register for signal <delayPipeline\_8767>.

Found 14-bit shift register for signal <delayPipeline\_8753>.

Found 14-bit shift register for signal <delayPipeline\_8736>.

Found 14-bit shift register for signal <delayPipeline\_8721>.

Found 14-bit shift register for signal <delayPipeline\_8704>.

Found 449-bit shift register for signal <delayPipeline\_8255>.

Found 15-bit shift register for signal <delayPipeline\_8240>.

Found 15-bit shift register for signal <delayPipeline\_8224>.

Found 15-bit shift register for signal <delayPipeline\_8208>.

Found 15-bit shift register for signal <delayPipeline\_8192>.

Found 449-bit shift register for signal <delayPipeline\_7743>.

Found 15-bit shift register for signal <delayPipeline\_7728>.

Found 15-bit shift register for signal <delayPipeline\_7712>.

Found 15-bit shift register for signal <delayPipeline\_7696>.

Found 15-bit shift register for signal <delayPipeline\_7680>.

Found 449-bit shift register for signal <delayPipeline\_7231>.

Found 14-bit shift register for signal <delayPipeline\_7217>.

Found 14-bit shift register for signal <delayPipeline\_7200>.

Found 14-bit shift register for signal <delayPipeline\_7185>.

Found 14-bit shift register for signal <delayPipeline\_7168>.

Found 449-bit shift register for signal <delayPipeline\_6719>.

Found 13-bit shift register for signal <delayPipeline\_6706>.

Found 5-bit shift register for signal <delayPipeline\_6701>.

Found 13-bit shift register for signal <delayPipeline\_6688>.

Found 13-bit shift register for signal <delayPipeline\_6674>.

Found 5-bit shift register for signal <delayPipeline\_6669>.

Found 13-bit shift register for signal <delayPipeline\_6656>.

Found 449-bit shift register for signal <delayPipeline\_6207>.

Found 12-bit shift register for signal <delayPipeline\_6195>.

Found 7-bit shift register for signal <delayPipeline\_6188>.

Found 12-bit shift register for signal <delayPipeline\_6176>.

Found 12-bit shift register for signal <delayPipeline\_6163>.

Found 7-bit shift register for signal <delayPipeline\_6156>.

Found 12-bit shift register for signal <delayPipeline\_6144>.

Found 449-bit shift register for signal <delayPipeline\_5695>.

Found 11-bit shift register for signal <delayPipeline\_5684>.

Found 9-bit shift register for signal <delayPipeline\_5675>.

Found 11-bit shift register for signal <delayPipeline\_5664>.

Found 11-bit shift register for signal <delayPipeline\_5652>.

Found 9-bit shift register for signal <delayPipeline\_5643>.

Found 11-bit shift register for signal <delayPipeline\_5632>.

Found 449-bit shift register for signal <delayPipeline\_5183>.

Found 10-bit shift register for signal <delayPipeline\_5173>.

Found 11-bit shift register for signal <delayPipeline\_5162>.

Found 10-bit shift register for signal <delayPipeline\_5152>.

Found 10-bit shift register for signal <delayPipeline\_5141>.

Found 11-bit shift register for signal <delayPipeline\_5130>.

Found 10-bit shift register for signal <delayPipeline\_5120>.

Found 449-bit shift register for signal <delayPipeline\_4671>.

Found 9-bit shift register for signal <delayPipeline\_4662>.

Found 13-bit shift register for signal <delayPipeline\_4649>.

Found 9-bit shift register for signal <delayPipeline\_4640>.

Found 9-bit shift register for signal <delayPipeline\_4630>.

Found 13-bit shift register for signal <delayPipeline\_4617>.

Found 9-bit shift register for signal <delayPipeline\_4608>.

Found 449-bit shift register for signal <delayPipeline\_4159>.

Found 8-bit shift register for signal <delayPipeline\_4151>.

Found 15-bit shift register for signal <delayPipeline\_4136>.

Found 8-bit shift register for signal <delayPipeline\_4128>.

Found 8-bit shift register for signal <delayPipeline\_4119>.

Found 15-bit shift register for signal <delayPipeline\_4104>.

Found 8-bit shift register for signal <delayPipeline\_4096>.

Found 450-bit shift register for signal <delayPipeline\_3646>.

Found 6-bit shift register for signal <delayPipeline\_3640>.

Found 17-bit shift register for signal <delayPipeline\_3623>.

Found 6-bit shift register for signal <delayPipeline\_3617>.

Found 6-bit shift register for signal <delayPipeline\_3608>.

Found 17-bit shift register for signal <delayPipeline\_3591>.

Found 6-bit shift register for signal <delayPipeline\_3585>.

Found 452-bit shift register for signal <delayPipeline\_3133>.

Found 4-bit shift register for signal <delayPipeline\_3129>.

Found 19-bit shift register for signal <delayPipeline\_3110>.

Found 4-bit shift register for signal <delayPipeline\_3106>.

Found 5-bit shift register for signal <delayPipeline\_3101>.

Found 4-bit shift register for signal <delayPipeline\_3097>.

Found 19-bit shift register for signal <delayPipeline\_3078>.

Found 4-bit shift register for signal <delayPipeline\_3074>.

Found 454-bit shift register for signal <delayPipeline\_2620>.

Found 21-bit shift register for signal <delayPipeline\_2597>.

Found 7-bit shift register for signal <delayPipeline\_2588>.

Found 21-bit shift register for signal <delayPipeline\_2565>.

Found 456-bit shift register for signal <delayPipeline\_2107>.

Found 23-bit shift register for signal <delayPipeline\_2084>.

Found 9-bit shift register for signal <delayPipeline\_2075>.

Found 23-bit shift register for signal <delayPipeline\_2052>.

Found 458-bit shift register for signal <delayPipeline\_1594>.

Found 21-bit shift register for signal <delayPipeline\_1573>.

Found 11-bit shift register for signal <delayPipeline\_1562>.

Found 21-bit shift register for signal <delayPipeline\_1541>.

Found 460-bit shift register for signal <delayPipeline\_1081>.

Found 19-bit shift register for signal <delayPipeline\_1062>.

Found 13-bit shift register for signal <delayPipeline\_1049>.

Found 19-bit shift register for signal <delayPipeline\_1030>.

Found 462-bit shift register for signal <delayPipeline\_568>.

Found 17-bit shift register for signal <delayPipeline\_551>.

Found 15-bit shift register for signal <delayPipeline\_536>.

Found 17-bit shift register for signal <delayPipeline\_519>.

Found 464-bit shift register for signal <delayPipeline\_55>.

Found 17-bit shift register for signal <delayPipeline\_23>.

Unit <Houghtransform> processed.

=========================================================================

Final Register Report

Macro Statistics

# Registers : 238

Flip-Flops : 238

# Shift Registers : 356

10-bit shift register : 16

11-bit shift register : 28

12-bit shift register : 16

13-bit shift register : 28

14-bit shift register : 16

15-bit shift register : 28

17-bit shift register : 20

19-bit shift register : 16

21-bit shift register : 16

23-bit shift register : 8

4-bit shift register : 16

449-bit shift register : 30

450-bit shift register : 4

452-bit shift register : 4

454-bit shift register : 4

456-bit shift register : 4

458-bit shift register : 4

460-bit shift register : 4

462-bit shift register : 4

464-bit shift register : 4

465-bit shift register : 1

5-bit shift register : 12

6-bit shift register : 16

7-bit shift register : 12

8-bit shift register : 16

9-bit shift register : 29

=========================================================================

=========================================================================

\* Partition Report \*

=========================================================================

Partition Implementation Status

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No Partitions were found in this design.

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=========================================================================

\* Final Report \*

=========================================================================

Clock Information:

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-----------------------------------+------------------------+-------+

Clock Signal | Clock buffer(FF name) | Load |

-----------------------------------+------------------------+-------+

clk | BUFGP | 2618 |

-----------------------------------+------------------------+-------+

Asynchronous Control Signals Information:

----------------------------------------

-----------------------------------+------------------------+-------+

Control Signal | Buffer(FF name) | Load |

-----------------------------------+------------------------+-------+

reset | BUFGP | 1058 |

-----------------------------------+------------------------+-------+

Timing Summary:

---------------

Speed Grade: -3

Minimum period: 163.048ns (Maximum Frequency: 6.133MHz)

Minimum input arrival time before clock: 1.338ns

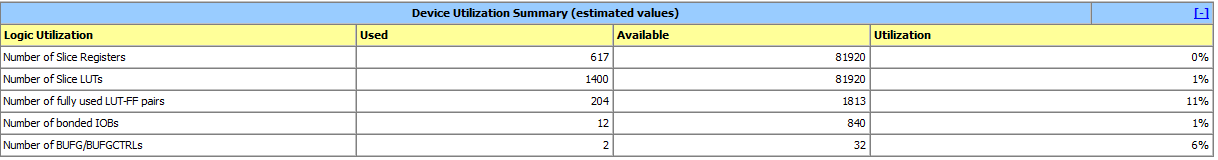
Maximum output required time after clock: 2.775ns

Maximum combinational path delay: No path found

=========================================================================

Process "Synthesize - XST" completed successfully

# 128\*384, Kreis mit Kreuz



Started : "Synthesize - XST".

Running xst...

Command Line: xst -intstyle ise -ifn "C:/Users/frank.schumacher/Merses/Work/VHDL/Correlation\_ShiftPipeline15052012/Houghtransform.xst" -ofn "C:/Users/frank.schumacher/Merses/Work/VHDL/Correlation\_ShiftPipeline15052012/Houghtransform.syr"

Reading design: Houghtransform.prj

=========================================================================

\* HDL Compilation \*

=========================================================================

Compiling vhdl file "C:/Users/frank.schumacher/Merses/Work/VHDL/Correlation\_ShiftPipeline15052012/source/imagedata.vhd" in Library work.

Package <testimage> compiled.

Compiling vhdl file "C:/Users/frank.schumacher/Merses/Work/VHDL/Correlation\_ShiftPipeline15052012/source/maskdata.vhd" in Library work.

Package <maskdata> compiled.

Compiling vhdl file "C:/Users/frank.schumacher/Merses/Work/VHDL/Correlation\_ShiftPipeline15052012/source/referencedata.vhd" in Library work.

Package <referencedata> compiled.

Compiling vhdl file "C:/Users/frank.schumacher/Merses/Work/VHDL/Correlation\_ShiftPipeline15052012/source/topx0.vhd" in Library work.

Architecture behavioral of Entity houghtransform is up to date.

=========================================================================

\* Design Hierarchy Analysis \*

=========================================================================

Analyzing hierarchy for entity <Houghtransform> in library <work> (architecture <behavioral>).

=========================================================================

\* HDL Analysis \*

=========================================================================

Analyzing Entity <Houghtransform> in library <work> (Architecture <behavioral>).

Entity <Houghtransform> analyzed. Unit <Houghtransform> generated.

=========================================================================

\* HDL Synthesis \*

=========================================================================

Performing bidirectional port resolution...

Synthesizing Unit <Houghtransform>.

Related source file is "C:/Users/frank.schumacher/Merses/Work/VHDL/Correlation\_ShiftPipeline15052012/source/topx0.vhd".

WARNING:Xst:1780 - Signal <pixOut\_sig\_next> is never used or assigned. This unconnected signal will be trimmed during the optimization process.

WARNING:Xst:646 - Signal <delayPipeline<0><0>> is assigned but never used. This unconnected signal will be trimmed during the optimization process.

Found 8-bit register for signal <pixOut>.

Found 11935-bit register for signal <delayPipeline<1:11935>>.

Found 8-bit adder for signal <pixOut\_sig>.

Found 8-bit adder for signal <pixOut\_sig$addsub0000> created at line 68.

Found 8-bit adder for signal <pixOut\_sig$addsub0001> created at line 68.

Found 8-bit adder for signal <pixOut\_sig$addsub0002> created at line 68.

Found 8-bit adder for signal <pixOut\_sig$addsub0003> created at line 68.

Found 8-bit adder for signal <sum$add0000> created at line 68.

Found 8-bit adder for signal <sum$add0001> created at line 68.

Found 8-bit adder for signal <sum$add0002> created at line 68.

Found 8-bit adder for signal <sum$add0003> created at line 68.

Found 8-bit adder for signal <sum$add0004> created at line 68.

Found 8-bit adder for signal <sum$add0005> created at line 68.

Found 8-bit adder for signal <sum$add0006> created at line 68.

Found 8-bit adder for signal <sum$add0007> created at line 68.

Found 8-bit adder for signal <sum$add0008> created at line 68.

Found 8-bit adder for signal <sum$add0009> created at line 68.

Found 8-bit adder for signal <sum$add0010> created at line 68.

Found 8-bit adder for signal <sum$add0011> created at line 68.

Found 8-bit adder for signal <sum$add0012> created at line 68.

Found 8-bit adder for signal <sum$addsub0000> created at line 68.

Found 8-bit adder for signal <sum$addsub0001> created at line 68.

Found 8-bit adder for signal <sum$addsub0002> created at line 68.

Found 8-bit adder for signal <sum$addsub0003> created at line 68.

Found 8-bit adder for signal <sum$addsub0004> created at line 68.

Found 8-bit adder for signal <sum$addsub0005> created at line 68.

Found 8-bit adder for signal <sum$addsub0006> created at line 68.

Found 8-bit adder for signal <sum$addsub0007> created at line 68.

Found 8-bit adder for signal <sum$addsub0008> created at line 68.

Found 8-bit adder for signal <sum$addsub0009> created at line 68.

Found 8-bit adder for signal <sum$addsub0010> created at line 68.

Found 8-bit adder for signal <sum$addsub0011> created at line 68.

Found 8-bit adder for signal <sum$addsub0012> created at line 68.

Found 8-bit adder for signal <sum$addsub0013> created at line 68.

Found 8-bit adder for signal <sum$addsub0014> created at line 68.

Found 8-bit adder for signal <sum$addsub0015> created at line 68.

Found 8-bit adder for signal <sum$addsub0016> created at line 68.

Found 8-bit adder for signal <sum$addsub0017> created at line 68.

Found 8-bit adder for signal <sum$addsub0018> created at line 68.

Found 8-bit adder for signal <sum$addsub0019> created at line 68.

Found 8-bit adder for signal <sum$addsub0020> created at line 68.

Found 8-bit adder for signal <sum$addsub0021> created at line 68.

Found 8-bit adder for signal <sum$addsub0022> created at line 68.

Found 8-bit adder for signal <sum$addsub0023> created at line 68.

Found 8-bit adder for signal <sum$addsub0024> created at line 68.

Found 8-bit adder for signal <sum$addsub0025> created at line 68.

Found 8-bit adder for signal <sum$addsub0026> created at line 68.

Found 8-bit adder for signal <sum$addsub0027> created at line 68.

Found 8-bit adder for signal <sum$addsub0028> created at line 68.

Found 8-bit adder for signal <sum$addsub0029> created at line 68.

created at line 68.

Found 8-bit adder for signal <sum$addsub0031> created at line 68.

Found 8-bit adder for signal <sum$addsub0032> created at line 68.

Found 8-bit adder for signal <sum$addsub0033> created at line 68.

Found 8-bit adder for signal <sum$addsub0034> created at line 68.

Found 8-bit adder for signal <sum$addsub0035> created at line 68.

Found 8-bit adder for signal <sum$addsub0036> created at line 68.

Found 8-bit adder for signal <sum$addsub0037> created at line 68.

Found 8-bit adder for signal <sum$addsub0038> created at line 68.

Found 8-bit adder for signal <sum$addsub0039> created at line 68.

Found 8-bit adder for signal <sum$addsub0040> created at line 68.

Found 8-bit adder for signal <sum$addsub0041> created at line 68.

Found 8-bit adder for signal <sum$addsub0042> created at line 68.

Found 8-bit adder for signal <sum$addsub0043> created at line 68.

Found 8-bit adder for signal <sum$addsub0044> created at line 68.

Found 8-bit adder for signal <sum$addsub0045> created at line 68.

Found 8-bit adder for signal <sum$addsub0046> created at line 68.

Found 8-bit adder for signal <sum$addsub0047> created at line 68.

Found 8-bit adder for signal <sum$addsub0048> created at line 68.

Found 8-bit adder for signal <sum$addsub0049> created at line 68.

Found 8-bit adder for signal <sum$addsub0050> created at line 68.

Found 8-bit adder for signal <sum$addsub0051> created at line 68.

Found 8-bit adder for signal <sum$addsub0052> created at line 68.

Found 8-bit adder for signal <sum$addsub0053> created at line 68.

Found 8-bit adder for signal <sum$addsub0054> created at line 68.

Found 8-bit adder for signal <sum$addsub0055> created at line 68.

Found 8-bit adder for signal <sum$addsub0056> created at line 68.

Found 8-bit adder for signal <sum$addsub0057> created at line 68.

Found 8-bit adder for signal <sum$addsub0058> created at line 68.

Found 8-bit adder for signal <sum$addsub0059> created at line 68.

Found 8-bit adder for signal <sum$addsub0060> created at line 68.

Found 8-bit adder for signal <sum$addsub0061> created at line 68.

Found 8-bit adder for signal <sum$addsub0062> created at line 68.

Found 8-bit adder for signal <sum$addsub0063> created at line 68.

Found 8-bit adder for signal <sum$addsub0064> created at line 68.

Found 8-bit adder for signal <sum$addsub0065> created at line 68.

Found 8-bit adder for signal <sum$addsub0066> created at line 68.

Found 8-bit adder for signal <sum$addsub0067> created at line 68.

Found 8-bit adder for signal <sum$addsub0068> created at line 68.

Found 8-bit adder for signal <sum$addsub0069> created at line 68.

Found 8-bit adder for signal <sum$addsub0070> created at line 68.

Found 8-bit adder for signal <sum$addsub0071> created at line 68.

Found 8-bit adder for signal <sum$addsub0030>.

Found 8-bit adder for signal <sum$addsub0073> created at line 68.

Found 8-bit adder for signal <sum$addsub0074> created at line 68.

Found 8-bit adder for signal <sum$addsub0075> created at line 68.

Found 8-bit adder for signal <sum$addsub0076> created at line 68.

Found 8-bit adder for signal <sum$addsub0077> created at line 68.

Found 8-bit adder for signal <sum$addsub0078> created at line 68.

Found 8-bit adder for signal <sum$addsub0079> created at line 68.

Found 8-bit adder for signal <sum$addsub0080> created at line 68.

Found 8-bit adder for signal <sum$addsub0081> created at line 68.

Found 8-bit adder for signal <sum$addsub0082> created at line 68.

Found 8-bit adder for signal <sum$addsub0083> created at line 68.

Found 8-bit adder for signal <sum$addsub0084> created at line 68.

Found 8-bit adder for signal <sum$addsub0085> created at line 68.

Found 8-bit adder for signal <sum$addsub0086> created at line 68.

Found 8-bit adder for signal <sum$addsub0087> created at line 68.

Found 8-bit adder for signal <sum$addsub0088> created at line 68.

Found 8-bit adder for signal <sum$addsub0089> created at line 68.

Found 8-bit adder for signal <sum$addsub0090> created at line 68.

Found 8-bit adder for signal <sum$addsub0091> created at line 68.

Found 8-bit adder for signal <sum$addsub0092> created at line 68.

Found 8-bit adder for signal <sum$addsub0093> created at line 68.

Found 8-bit adder for signal <sum$addsub0094> created at line 68.

Found 8-bit adder for signal <sum$addsub0095> created at line 68.

Found 8-bit adder for signal <sum$addsub0096> created at line 68.

Found 8-bit adder for signal <sum$addsub0097> created at line 68.

Found 8-bit adder for signal <sum$addsub0098> created at line 68.

Found 8-bit adder for signal <sum$addsub0099> created at line 68.

Found 8-bit adder for signal <sum$addsub0100> created at line 68.

Found 8-bit adder for signal <sum$addsub0101> created at line 68.

Found 8-bit adder for signal <sum$addsub0102> created at line 68.

Found 8-bit adder for signal <sum$addsub0103> created at line 68.

Found 8-bit adder for signal <sum$addsub0104> created at line 68.

Found 8-bit adder for signal <sum$addsub0105> created at line 68.

Found 8-bit adder for signal <sum$addsub0106> created at line 68.

Found 8-bit adder for signal <sum$addsub0107> created at line 68.

Found 8-bit adder for signal <sum$addsub0108> created at line 68.

Found 8-bit adder for signal <sum$addsub0109> created at line 68.

Found 8-bit adder for signal <sum$addsub0110> created at line 68.

Found 8-bit adder for signal <sum$addsub0111> created at line 68.

Found 8-bit adder for signal <sum$addsub0112> created at line 68.

Found 8-bit adder for signal <sum$addsub0072> created at line 68 Found 8-bit adder for signal <sum$addsub0113> created at line 68.

Found 8-bit adder for signal <sum$addsub0114> created at line 68.

Found 8-bit adder for signal <sum$addsub0115> created at line 68.

Found 8-bit adder for signal <sum$addsub0116> created at line 68.

INFO:Xst:738 - HDL ADVISOR - 11935 flip-flops were inferred for signal <delayPipeline>. You may be trying to describe a RAM in a way that is incompatible with block and distributed RAM resources available on Xilinx devices, or with a specific template that is not supported. Please review the Xilinx resources documentation and the XST user manual for coding guidelines. Taking advantage of RAM resources will lead to improved device usage and reduced synthesis time.

Summary:

inferred 11943 D-type flip-flop(s).

inferred 135 Adder/Subtractor(s).

Unit <Houghtransform> synthesized.

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HDL Synthesis Report

Macro Statistics

# Adders/Subtractors : 135

8-bit adder : 135

# Registers : 11929

1-bit register : 11928

8-bit register : 1

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\* Advanced HDL Synthesis \*

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Advanced HDL Synthesis Report

Macro Statistics

# Adders/Subtractors : 134

8-bit adder : 133

8-bit adder carry in : 1

# Registers : 11936

Flip-Flops : 11936

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\* Low Level Synthesis \*

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Optimizing unit <Houghtransform> ...

Mapping all equations...

Building and optimizing final netlist ...

Found area constraint ratio of 100 (+ 5) on block Houghtransform, actual ratio is 21.

Final Macro Processing ...

Processing Unit <Houghtransform> :

Found 9-bit shift register for signal <delayPipeline\_11927>.

Found 368-bit shift register for signal <delayPipeline\_11544>.

Found 17-bit shift register for signal <delayPipeline\_11527>.

Found 366-bit shift register for signal <delayPipeline\_11161>.

Found 19-bit shift register for signal <delayPipeline\_11142>.

Found 364-bit shift register for signal <delayPipeline\_10778>.

Found 21-bit shift register for signal <delayPipeline\_10757>.

Found 362-bit shift register for signal <delayPipeline\_10395>.

Found 23-bit shift register for signal <delayPipeline\_10372>.

Found 360-bit shift register for signal <delayPipeline\_10012>.

Found 21-bit shift register for signal <delayPipeline\_9989>.

Found 358-bit shift register for signal <delayPipeline\_9629>.

Found 4-bit shift register for signal <delayPipeline\_9625>.

Found 19-bit shift register for signal <delayPipeline\_9606>.

Found 4-bit shift register for signal <delayPipeline\_9602>.

Found 356-bit shift register for signal <delayPipeline\_9246>.

Found 6-bit shift register for signal <delayPipeline\_9240>.

Found 17-bit shift register for signal <delayPipeline\_9223>.

Found 6-bit shift register for signal <delayPipeline\_9217>.

Found 354-bit shift register for signal <delayPipeline\_8863>.

Found 8-bit shift register for signal <delayPipeline\_8855>.

Found 15-bit shift register for signal <delayPipeline\_8840>.

Found 8-bit shift register for signal <delayPipeline\_8832>.

Found 353-bit shift register for signal <delayPipeline\_8479>.

Found 9-bit shift register for signal <delayPipeline\_8470>.

Found 13-bit shift register for signal <delayPipeline\_8457>.

Found 9-bit shift register for signal <delayPipeline\_8448>.

Found 353-bit shift register for signal <delayPipeline\_8095>.

Found 10-bit shift register for signal <delayPipeline\_8085>.

Found 11-bit shift register for signal <delayPipeline\_8074>.

Found 10-bit shift register for signal <delayPipeline\_8064>.

Found 353-bit shift register for signal <delayPipeline\_7711>.

Found 11-bit shift register for signal <delayPipeline\_7700>.

Found 9-bit shift register for signal <delayPipeline\_7691>.

Found 11-bit shift register for signal <delayPipeline\_7680>.

Found 353-bit shift register for signal <delayPipeline\_7327>.

Found 12-bit shift register for signal <delayPipeline\_7315>.

Found 7-bit shift register for signal <delayPipeline\_7308>.

Found 12-bit shift register for signal <delayPipeline\_7296>.

Found 353-bit shift register for signal <delayPipeline\_6943>.

Found 13-bit shift register for signal <delayPipeline\_6930>.

Found 5-bit shift register for signal <delayPipeline\_6925>.

Found 13-bit shift register for signal <delayPipeline\_6912>.

Found 353-bit shift register for signal <delayPipeline\_6559>.

Found 14-bit shift register for signal <delayPipeline\_6545>.

Found 14-bit shift register for signal <delayPipeline\_6528>.

Found 353-bit shift register for signal <delayPipeline\_6175>.

Found 15-bit shift register for signal <delayPipeline\_6160>.

Found 15-bit shift register for signal <delayPipeline\_6144>.

Found 353-bit shift register for signal <delayPipeline\_5791>.

Found 15-bit shift register for signal <delayPipeline\_5776>.

Found 15-bit shift register for signal <delayPipeline\_5760>.

Found 353-bit shift register for signal <delayPipeline\_5407>.

Found 14-bit shift register for signal <delayPipeline\_5393>.

Found 14-bit shift register for signal <delayPipeline\_5376>.

Found 353-bit shift register for signal <delayPipeline\_5023>.

Found 13-bit shift register for signal <delayPipeline\_5010>.

Found 5-bit shift register for signal <delayPipeline\_5005>.

Found 13-bit shift register for signal <delayPipeline\_4992>.

Found 353-bit shift register for signal <delayPipeline\_4639>.

Found 12-bit shift register for signal <delayPipeline\_4627>.

Found 7-bit shift register for signal <delayPipeline\_4620>.

Found 12-bit shift register for signal <delayPipeline\_4608>.

Found 353-bit shift register for signal <delayPipeline\_4255>.

Found 11-bit shift register for signal <delayPipeline\_4244>.

Found 9-bit shift register for signal <delayPipeline\_4235>.

Found 11-bit shift register for signal <delayPipeline\_4224>.

Found 353-bit shift register for signal <delayPipeline\_3871>.

Found 10-bit shift register for signal <delayPipeline\_3861>.

Found 11-bit shift register for signal <delayPipeline\_3850>.

Found 10-bit shift register for signal <delayPipeline\_3840>.

Found 353-bit shift register for signal <delayPipeline\_3487>.

Found 9-bit shift register for signal <delayPipeline\_3478>.

Found 13-bit shift register for signal <delayPipeline\_3465>.

Found 9-bit shift register for signal <delayPipeline\_3456>.

Found 353-bit shift register for signal <delayPipeline\_3103>.

Found 8-bit shift register for signal <delayPipeline\_3095>.

Found 15-bit shift register for signal <delayPipeline\_3080>.

Found 8-bit shift register for signal <delayPipeline\_3072>.

Found 354-bit shift register for signal <delayPipeline\_2718>.

Found 6-bit shift register for signal <delayPipeline\_2712>.

Found 17-bit shift register for signal <delayPipeline\_2695>.

Found 6-bit shift register for signal <delayPipeline\_2689>.

Found 356-bit shift register for signal <delayPipeline\_2333>.

Found 4-bit shift register for signal <delayPipeline\_2329>.

Found 19-bit shift register for signal <delayPipeline\_2310>.

Found 4-bit shift register for signal <delayPipeline\_2306>.

Found 358-bit shift register for signal <delayPipeline\_1948>.

Found 21-bit shift register for signal <delayPipeline\_1925>.

Found 360-bit shift register for signal <delayPipeline\_1563>.

Found 23-bit shift register for signal <delayPipeline\_1540>.

Found 362-bit shift register for signal <delayPipeline\_1178>.

Found 21-bit shift register for signal <delayPipeline\_1157>.

Found 364-bit shift register for signal <delayPipeline\_793>.

Found 19-bit shift register for signal <delayPipeline\_774>.

Found 366-bit shift register for signal <delayPipeline\_408>.

Found 17-bit shift register for signal <delayPipeline\_391>.

Found 368-bit shift register for signal <delayPipeline\_23>.

Unit <Houghtransform> processed.

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Final Register Report

Macro Statistics

# Registers : 54

Flip-Flops : 54

# Shift Registers : 98

10-bit shift register : 4

11-bit shift register : 6

12-bit shift register : 4

13-bit shift register : 6

14-bit shift register : 4

15-bit shift register : 6

17-bit shift register : 4

19-bit shift register : 4

21-bit shift register : 4

23-bit shift register : 2

353-bit shift register : 15

354-bit shift register : 2

356-bit shift register : 2

358-bit shift register : 2

360-bit shift register : 2

362-bit shift register : 2

364-bit shift register : 2

366-bit shift register : 2

368-bit shift register : 2

4-bit shift register : 4

5-bit shift register : 2

6-bit shift register : 4

7-bit shift register : 2

8-bit shift register : 4

9-bit shift register : 7

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\* Partition Report \*

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Partition Implementation Status

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No Partitions were found in this design.

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\* Final Report \*

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Clock Information:

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Clock Signal | Clock buffer(FF name) | Load |

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clk | BUFGP | 1039 |

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Asynchronous Control Signals Information:

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Control Signal | Buffer(FF name) | Load |

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reset | BUFGP | 519 |

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Timing Summary:

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Speed Grade: -3

Minimum period: 12.530ns (Maximum Frequency: 79.812MHz)

Minimum input arrival time before clock: 1.338ns

Maximum output required time after clock: 2.775ns

Maximum combinational path delay: No path found

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Process "Synthesize - XST" completed successfully